COM Express Carrier Design Guide

Carrier design guideline for

PCOM-B656VGL

Rev. R1.0

Revision history

Rev.	Date	Note
R0.1	29th.July.2021	1st Draft
R0.2	30th.July.2021	Update Table 1 PCOM-B656VGL Pin-Out
R0.3	26th. October.2021	Update Table 4 PCIE carrier available traces - Device Down Table 5 PCIE carrier available traces - Add In Card Table 6 PEG carrier available traces - Device Down Table 7 PEG carrier available traces - Add In Card Table 11 Carrier available traces - USB 2.0 / 3.0 Table 19 Carrier available traces - DDI Table 22 Carrier available traces - LAN Table 25 Carrier available traces - SATA Table 28 Carrier available traces – LVDS Channel A Table 29 Carrier available traces – LVDS Channel B
R1.0	2nd . August.2022	Correct pinout table

Contents

List of Tables

List of Figures

1 Introduction

The Carrier Design Guide provides the guideline of designing your own carrier board based on Portwell's COM Express Modular product PCOM-B656VGL. PCOM-B656VGL is Type 6, 125x95mm Modular board, more information is included in PCOM-B656VGL User's Guide and can be downloaded from Portwell download center (Or contact your Portwell sales representative for acquiring PCOM-B656VGL User's Guide). This carrier design guide is dedicated for the designers designing a COM Express Type 6 carrier board which will have a excellent compatibility with Portwell's PCOM-B656VGL modular product.

The layout guideline provided are 8 PCB layer stack up, each interface has three sections, which are detail PCOM-B656VGL pin out, pin name, power rail, PU/PD, AC couple capacitor and etc. information are included. Second part contains PCB layout guide, impedance, maximum trace, trace width, and trace spacing etc. Third section provides the available trace length of which designers are able to optimize the high speed signals such as PCIE, SATA, USB etc.

2 PCOM-B656VGL

2.1 PCOM-B656VGL Block Diagram

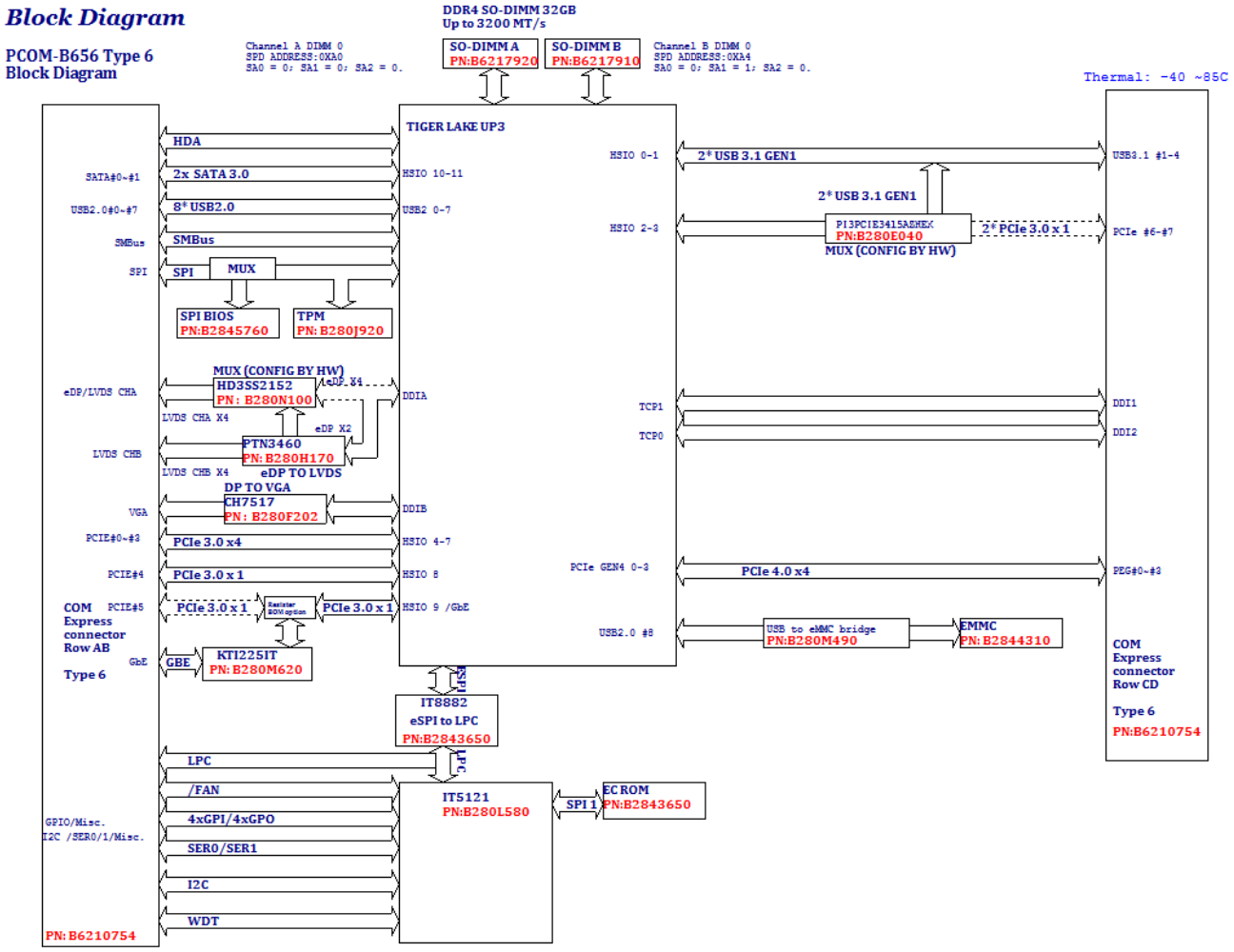


Figure 1 PCOM-B656VGL Block Diagram

2.2 PCOM-B656VGL Pin-out

Pin	Row A	Row B	Row C	Row D
1	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#	GND	GND
3	GBE0_MDI3+	LPC_FRAME#/ESPI_CS0#	USB_SSRX0-	USB_SSTX0-
4	GBE0_LINK100#	LPC_AD0/ESPI_IO_0	USB_SSRX0+	USB_SSTX0+
5	GBE0_LINK1000#	LPC_AD1/ESPI_IO_1	GND	GND
6	GBE0_MDI2-	LPC_AD2/ESPI_IO_2	USB_SSRX1-	USB_SSTX1-
7	GBE0_MDI2+	LPC_AD3/ESPI_IO_3	USB_SSRX1+	USB_SSTX1+
8	GBE0_LINK#	LPC_DRQ0#/ESPI_ALERT0#(NC)	GND	GND
9	GBE0_MDI1-	LPC_DRQ1#/ESPI_ALERT1#(NC)	USB_SSRX2-	USB_SSTX2-
10	GBE0_MDI1+	LPC_CLK/ESPI_CK	USB_SSRX2+	USB_SSTX2+
11	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
12	GBE0_MDI0-	PWRBTN#	USB_SSRX3-	USB_SSTX3-
13	GBE0_MDI0+	SMB_CK	USB_SSRX3+	USB_SSTX3+
14	GBE0_CTREF	SMB_DAT	GND	GND
15	SUS_S3#	SMB_ALERT#	DDI1_PAIR6+(NC)	DDI1_CTRLCLK_AUX+
16	SATA0_TX+	SATA1_TX+	DDI1_PAIR6-(NC)	DDI1_CTRLDATA_AUX-
17	SATA0_TX-	SATA1_TX-	RSVD(NC)	RSVD(NC)
18	SUS_S4#	SUS_STAT#/ESPI_RESET#	RSVD(NC)	RSVD(NC)
19	SATA0_RX+	SATA1_RX+	PCIE_RX6+	PCIE_TX6+
20	SATA0_RX-	SATA1_RX-	PCIE_RX6-	PCIE_TX6-
21	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
22	SATA2_TX+(NC)	SATA3_TX+(NC)	PCIE_RX7+	PCIE_TX7+
23	SATA2_TX-(NC)	SATA3_TX-(NC)	PCIE_RX7-	PCIE_TX7-
24	SUS_S5#	PWR_OK	DDI1_HPD	RSVD(NC)
25	SATA2_RX+(NC)	SATA3_RX+(NC)	DDI1_PAIR4 +(NC)	RSVD(NC)
26	SATA2_RX-(NC)	SATA3_RX-(NC)	DDI1_PAIR4-(NC)	DDI1_PAIR0+
27	BATLOW#	WDT	RSVD(NC)	DDI1_PAIR0-
28	(S)ATA_ACT#	HDA_SDIN2	RSVD(NC)	RSVD(NC)
29	HDA_SYNC	HDA_SDIN1	DDI1_PAIR5+(NC)	DDI1_PAIR1+
30	HDA_RST#	HDA_SDIN0	DDI1_PAIR5-(NC)	DDI1_PAIR1-
31	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
32	HDA_BITCLK	SPKR	DDI2_CTRLCLK_AUX+	DDI1_PAIR2+
33	HDA_SDOUT	I2C_CK	DDI2_CTRLDATA_AUX-	DDI1_PAIR2-
34	BIOS_DIS0#/ESPI_SAFS	I2C_DAT	DDI2_DDC_AUX_SEL	DDI1_DDC_AUX_SEL

35	THRMTRIP#	THRM#	RSVD(NC)	RSVD(NC)
36	USB6-	USB7-	DDI3_CTRLCLK_AUX+(NC)	DDI1_PAIR3+
37	USB6+	USB7+	DDI3_CTRLDATA_AUX-(NC)	DDI1_PAIR3-
38	USB_6_7_OC#	USB_4_5_OC#	DDI3_DDC_AUX_SEL(NC)	RSVD(NC)
39	USB4-	USB5-	DDI3_PAIR0+(NC)	DDI2_PAIR0+
40	USB4+	USB5+	DDI3_PAIR0-(NC)	DDI2_PAIR0-
41	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
42	USB2-	USB3-	DDI3_PAIR1+(NC)	DDI2_PAIR1+
43	USB2+	USB3+	DDI3_PAIR1-(NC)	DDI2_PAIR1-
44	USB_2_3_OC#	USB_0_1_OC#	DDI3_HPD(NC)	DDI2_HPD
45	USB0-	USB1-	RSVD(NC)	RSVD(NC)
46	USB0+	USB1+	DDI3_PAIR2+(NC)	DDI2_PAIR2+
47	VCC_RTC	ESPI_EN#	DDI3_PAIR2-(NC)	DDI2_PAIR2-
48	RSVD[10]	USB0_HOST_PRSNT	RSVD(NC)	RSVD(NC)
49	GBE0_SDP	SYS_RESET#	DDI3_PAIR3+NC)	DDI2_PAIR3+
50	LPC_SERIRQ/ESPI_CS1#	CB_RESET#	DDI3_PAIR3-(NC)	DDI2_PAIR3-
51	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
52	PCIE_TX5+	PCIE_RX5+	PEG_RX0+	PEG_TX0+
53	PCIE_TX5-	PCIE_RX5-	PEG_RX0-	PEG_TX0-
54	GPI0	GPO1	TYPE0#	PEG_LANE_RV#
55	PCIE_TX4+	PCIE_RX4+	PEG_RX1+	PEG_TX1+
56	PCIE_TX4-	PCIE_RX4-	PEG_RX1-	PEG_TX1-
57	GND	GPO2	TYPE1#	TYPE2#
58	PCIE_TX3+	PCIE_RX3+	PEG_RX2+	PEG_TX2+
59	PCIE_TX3-	PCIE_RX3-	PEG_RX2-	PEG_TX2-
60	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
61	PCIE_TX2+	PCIE_RX2+	PEG_RX3+	PEG_TX3+
62	PCIE_TX2-	PCIE_RX2-	PEG_RX3-	PEG_TX3-
63	GPI1	GPO3	RSVD(NC)	RSVD(NC)
64	PCIE_TX1+	PCIE_RX1+	RSVD(NC)	RSVD(NC)
65	PCIE_TX1-	PCIE_RX1-	PEG_RX4+(NC)	PEG_TX4+(NC)
66	GND	WAKE0#	PEG_RX4-(NC)	PEG_TX4-(NC)
67	GPI2	WAKE1#(NC)	RAPID_SHUTDOWN	GND
68	PCIE_TX0+	PCIE_RX0+	PEG_RX5+(NC)	PEG_TX5+(NC)
69	PCIE_TX0-	PCIE_RX0-	PEG_RX5-(NC)	PEG_TX5-(NC)
70	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
71	LVDS_A0+	LVDS_B0+	PEG_RX6+(NC)	PEG_TX6+(NC)

72	LVDS_A0-	LVDS_B0-	PEG_RX6-(NC)	PEG_TX6-(NC)
73	LVDS_A1+	LVDS_B1+	GND	GND
74	LVDS_A1-	LVDS_B1-	PEG_RX7+(NC)	PEG_TX7+(NC)
75	LVDS_A2+	LVDS_B2+	PEG_RX7-(NC)	PEG_TX7-(NC)
76	LVDS_A2-	LVDS_B2-	GND	GND
77	LVDS_VDD_EN	LVDS_B3+	RSVD(NC)	RSVD(NC)
78	LVDS_A3+	LVDS_B3-	PEG_RX8+(NC)	PEG_TX8+(NC)
79	LVDS_A3-	LVDS_BKLT_EN	PEG_RX8-(NC)	PEG_TX8-(NC)
80	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
81	LVDS_A_CK+	LVDS_B_CK+	PEG_RX9+(NC)	PEG_TX9+(NC)
82	LVDS_A_CK-	LVDS_B_CK-	PEG_RX9-(NC)	PEG_TX9-(NC)
83	LVDS_I2C_CK	LVDS_BKLT_CTRL	RSVD(NC)	RSVD(NC)
84	LVDS_I2C_DAT	VCC_5V_SBY	GND	GND
85	GPI3	VCC_5V_SBY	PEG_RX10+(NC)	PEG_TX10+(NC)
86	RSVD(NC)	VCC_5V_SBY	PEG_RX10-(NC)	PEG_TX10-(NC)
87	eDP_HPD	VCC_5V_SBY	GND	GND
88	PCIE_CLK_REF+	BIOS_DIS1#	PEG_RX11+(NC)	PEG_TX11+(NC)
89	PCIE_CLK_REF-	VGA_RED	PEG_RX11-(NC)	PEG_TX11-(NC)
90	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
91	SPI_POWER	VGA_GRN	PEG_RX12+(NC)	PEG_TX12+(NC)
92	SPI_MISO	VGA_BLU	PEG_RX12-(NC)	PEG_TX12-(NC)
93	GPO0	VGA_HSYNC	GND	GND
94	SPI_CLK	VGA_VSYNC	PEG_RX13+(NC)	PEG_TX13+(NC)
95	SPI_MOSI	VGA_I2C_CK	PEG_RX13-(NC)	PEG_TX13-(NC)
96	TPM_PP	VGA_I2C_DAT	GND	GND
97	TYPE10#	SPI_CS#	RSVD(NC)	RSVD(NC)
98	SER0_TX	RSVD(NC)	PEG_RX14+(NC)	PEG_TX14+(NC)
99	SER0_RX	RSVD(NC)	PEG_RX14-(NC)	PEG_TX14-(NC)
100	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
101	SER1_TX	FAN_PWMOUT	PEG_RX15+(NC)	PEG_TX15+(NC)
102	SER1_RX	FAN_TACHIN	PEG_RX15-(NC)	PEG_TX15-(NC)
103	LID#	SLEEP#	GND	GND
104	VCC_12V	VCC_12V	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V	VCC_12V	VCC_12V

109	VCC_12V	VCC_12V	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

Table 2 PCOM-B656VGL Pin-Out

3 COM Express Interface

3.1 PCIe / PEG

PCOM-B656VGL PCIe

PCIE7	PCIE7	Module Pin-out Types 6,7	Bucket B1
PCIE6	PCIE6		
PCIE5	PCIE5	Module Pin-out Types 6,7	
PCIE4	PCIE4		
PCIE3	PCIE3	Module Pin-out Types 6,7,10	
PCIE2	PCIE2		
PCIE1	PCIE1		
PCIE0	PCIE0		

Table 1 PCOM-B656VGL PCIE for different types

Pin #	Pin NAME	COMe 3.0 Specification Signals Requiring Module Termination	Pin Typ	B656VGL Module	PWR Rail /Tolerance(Volt)
C52	PEG_RX0+	AC coupled off Module	I PCIe	AC coupled off module	AC coupled off module
C53	PEG_RX0-				
C55	PEG_RX1+				
C56	PEG_RX1-				
C58	PEG_RX2+				
C59	PEG_RX2-				
C61	PEG_RX3+				
C62	PEG_RX3-				
C65	PEG_RX4+			NC	NC
C66	PEG_RX4-				
C68	PEG_RX5+				
C69	PEG_RX5-				
C71	PEG_RX6+				
C72	PEG_RX6-				
C74	PEG_RX7+				
C75	PEG_RX7-				
C78	PEG_RX8+				
C79	PEG_RX8-				
C81	PEG_RX9+				
C82	PEG_RX9-				
C85	PEG_RX10+				
C86	PEG_RX10-				
C88	PEG_RX11+				
C89	PEG_RX11-				
C91	PEG_RX12+				
C92	PEG_RX12-				
C94	PEG_RX13+				
C95	PEG_RX13-				
C98	PEG_RX14+				
C99	PEG_RX14-				
C101	PEG_RX15+				
C102	PEG_RX15-				

Pin#	Pin Name	COMe 3.0 SPECIFICATION Signals Requiring Module Termination	Pin Typ	B656VGL Module	Pwr Rail/ Tolerance (Volt)
A48	N/C	-	O CMOS	RSVD Pin	3.3V/3.3V
A49	CPU_CFG5	Pulled-up to 3.3V on module with a 10k ohm resistor	I CMOS	PU 10K ohm to V3P3A.	3.3V/3.3V
A88	PCIE_CLK_REF+	-	O PCIE	PCH to COM Express Row connector.	PCIE
A89	PCIE_CLK_REF-	-	O PCIE	PCH to COM Express Row connector.	PCIE
B47	N/C	-	O CMOS	PU 10K ohm to V3P3A.	3.3V/3.3V
B48	CPU_CFG6	Pulled-up to 3.3V on module with a 10K ohm resistor	I CMOS	PU 10K ohm to V3P3A.	3.3V/3.3V
B50	CB_RESET#	Pulled-up to 3.3V on module with a 10K ohm resistor	O CMOS	EC to COM Express Row connector.	3.3V Suspend/3.3V
B66	WAKE0#	Pulled-up to 3.3V on module with a 10K ohm resistor	I CMOS	PCH to COM Express Row connector.	3.3V Suspend/3.3V

Table 2 PCOM-B656VGL PCIE/PEG

PCOM-B656VGL PEG

Pin #	Pin NAME	COMe 3.0 Specification Signals Requiring Module Termination	Pin Typ	B656VGL Module	PWR Rail /Tolerance(Volt)
C52	PEG_RX0+	AC coupled off Module	I PCIe	AC coupled off module	AC coupled off module
C53	PEG_RX0-				
C55	PEG_RX1+				
C56	PEG_RX1-				
C58	PEG_RX2+				
C59	PEG_RX2-				
C61	PEG_RX3+				
C62	PEG_RX3-				
C65	PEG_RX4+			NC	NC
C66	PEG_RX4-				
C68	PEG_RX5+				
C69	PEG_RX5-				
C71	PEG_RX6+				
C72	PEG_RX6-				
C74	PEG_RX7+				
C75	PEG_RX7-				
C78	PEG_RX8+				
C79	PEG_RX8-				
C81	PEG_RX9+				
C82	PEG_RX9-				
C85	PEG_RX10+				
C86	PEG_RX10-				
C88	PEG_RX11+				
C89	PEG_RX11-				
C91	PEG_RX12+				
C92	PEG_RX12-				
C94	PEG_RX13+				
C95	PEG_RX13-				
C98	PEG_RX14+				
C99	PEG_RX14-				
C101	PEG_RX15+				
C102	PEG_RX15-				

D52	PEG_TX0+	AC coupled on module	○ PCIe	0.22uF AC coupled on the module (Gen3)	AC coupled on module
D53	PEG_TX0-				
D55	PEG_TX1+				
D56	PEG_TX1-				
D58	PEG_TX2+				
D59	PEG_TX2-				
D61	PEG_TX3+				
D62	PEG_TX3-				
D65	PEG_TX4+			NC	NC
D66	PEG_TX4-				
D68	PEG_TX5+				
D69	PEG_TX5-				
D71	PEG_TX6+				
D72	PEG_TX6-				
D74	PEG_TX7+				
D75	PEG_TX7-				
D78	PEG_TX8+				
D79	PEG_TX8-				
D81	PEG_TX9+				
D82	PEG_TX9-				
D85	PEG_TX10+				
D86	PEG_TX10-				
D88	PEG_TX11+				
D89	PEG_TX11-				
D91	PEG_TX12+				
D92	PEG_TX12-				
D94	PEG_TX13+				
D95	PEG_TX13-				
D98	PEG_TX14+				
D99	PEG_TX14-				
D101	PEG_TX15+				
D102	PEG_TX15-				
D54	PEG_LANE_RV#		NC	NC	3.3V / 3.3V

Table 3 PCOM-B656VGL PEG

3.1.1 AC Coupling Capacitor

PCIE / PEG AC Coupling : Device Down

While PCIE devices are designed on COM Express Carrier Board, the AC coupling Capacitor should be added on the carrier, please refer to below diagram.

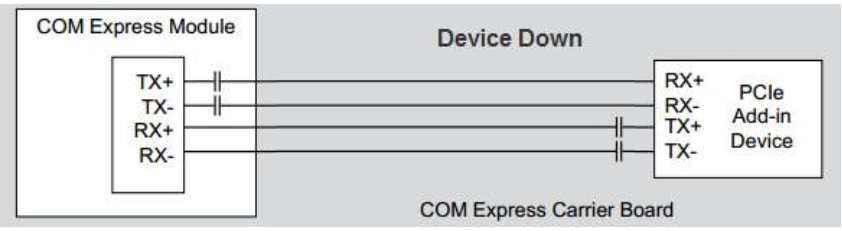


Figure 2 PCIE AC Coupling Capacitor - Device Down

(From PICMG COM Express Carrier Board Design Guide)

PCIE / PEG AC Coupling : Add-In Card

While PCIE devices are designed as Add In Card, the AC coupling Capacitor should be on PCIe Add-In Card, rather than on the COM Express Carrier Board, please refer to below

diagram.

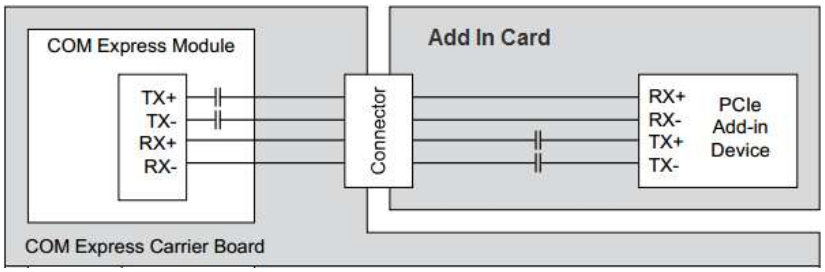


Figure 3 PCIE AC Coupling Capacitor - Add In Card

(From PICMG COM Express Carrier Board Design Guide)

3.1.2 PCB layout guideline - PCIe/PEG

Parameter	PCIe Gen1 / Gen2	PCIe Gen3	PEG Gen3
Bandwidth	2.5 G / 5 G	8 G	8 G
Maximum signal line length (coupled traces) TX and RX	12.0/10 inch	7/9 inch (Add In Card/ Device Down)	7/9 inch (Add In Card/ Device Down)
Differential impedance	85 Ω +/-15%	85 Ω +/-15%	85 Ω +/-15%
Single-ended Impedance	50 Ω +/-15%	50 Ω +/-15%	50 Ω +/-15%
Trace width (W)	3.5 mil PCB stack-up dependent	3.5 mil PCB stack-up dependent	3.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	15 mil PCB stack-up dependent	15 mil PCB stack-up dependent	15 mil PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Min. 15mils	Min. 15mils	Min. 15mils
Length matching between differential pairs (intra-pair)	Max. 5mils	Max. 5mils	Max. 5mils
Reference plane	GND referenced preferred	GND referenced preferred	GND referenced preferred
Spacing from edge of plane	Min. 10*W mils (W=trace width)	Min. 10*W mils (W=trace width)	Min. 10*W mils (W=trace width)
Via Usage	Max. 2 vias per TX trace Max. 2 vias per RX trace	Max. 1 vias per TX trace Max. 1 vias per RX trace	Max. 1 vias per TX trace Max.1 vias per RX trace

Table 3 PCIE/PEG Layout information

3.1.3 Passive Devices

AC Cap value (Gen1/Gen2)	Min = 75 nF Max = 265 nF	PCOM-B656VGL AC Cap value 220nF
AC Cap value (Gen3)	Min = 180nf Max = 265 nF	

Table 4 PCIE/PEG AC coupling capacitor value

3.1.4 Reference schematic - PCOM-C600 R0

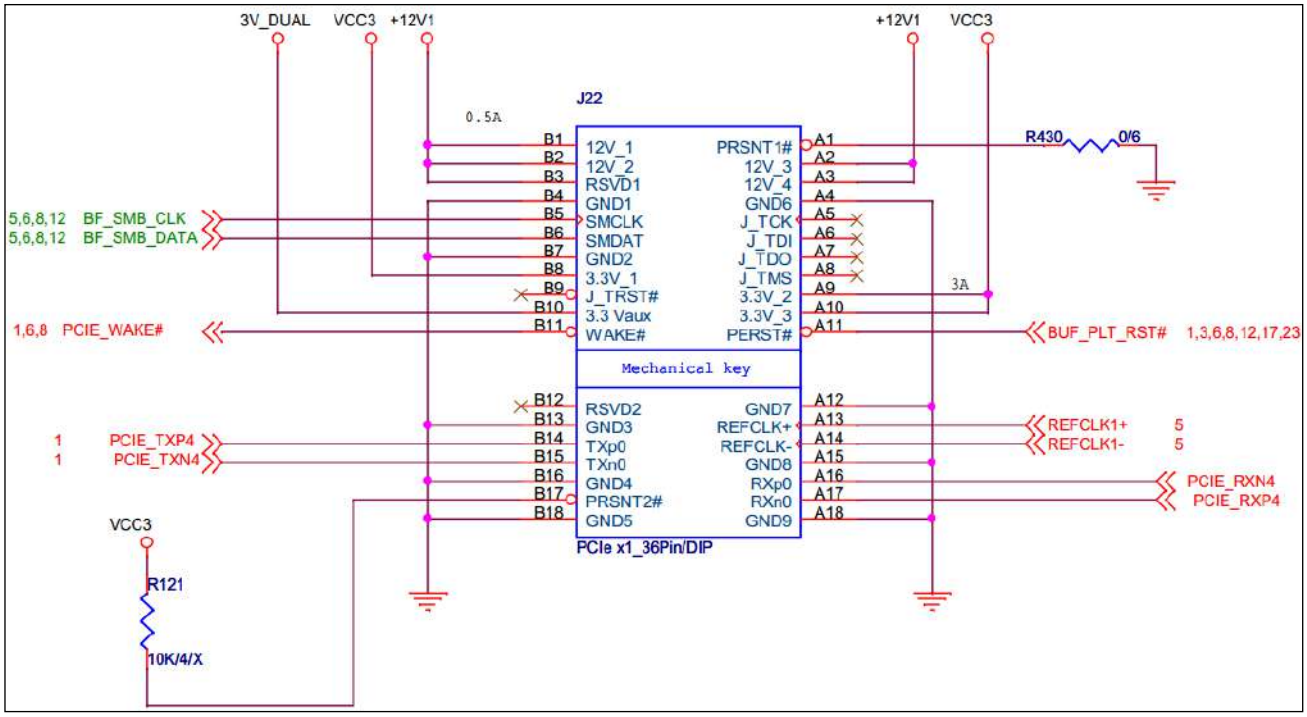


Figure 4 PCIE reference schematic

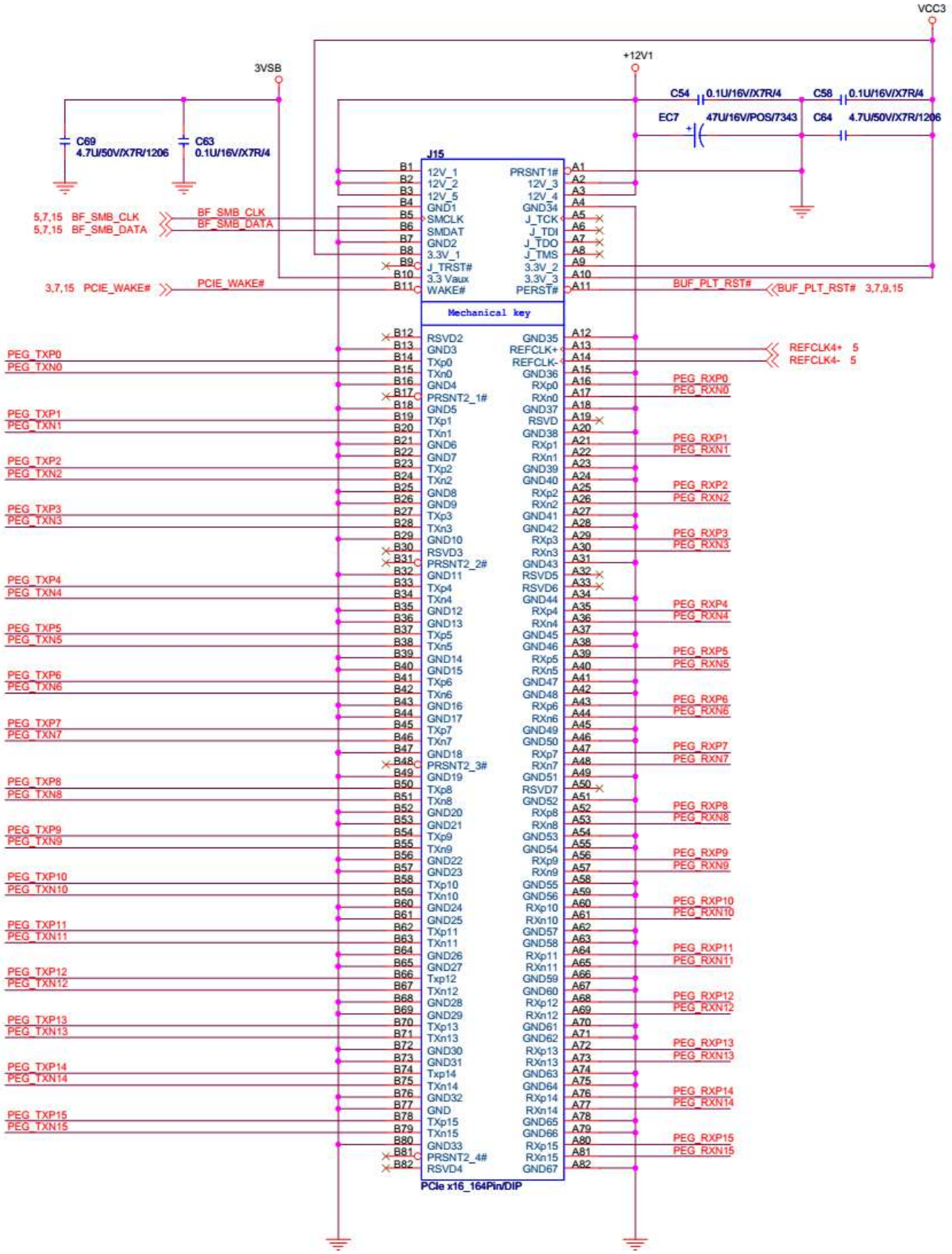


Figure 5 PEG reference schematic

3.1.5 Max trace length and available carrier trace length -

PCIe (Device Down)

PCIe Device Down Topology

PIN	Name	Module Length	Max Length	Available Carrier length (Device Down Topology)
B68	PCIE_RXP0	1187	9000	7813
B69	PCIE_RXN0	1184	9000	7816
A68	PCIE_TXN0	1639	9000	7361
A69	PCIE_TXP0	1638	9000	7362
B64	PCIE_RXN1	1285	9000	7715
B65	PCIE_RXP1	1285	9000	7715
A64	PCIE_TXN1	1628	9000	7372
A65	PCIE_TXP1	1628	9000	7372
B61	PCIE_RXN2	1229	9000	7771
B62	PCIE_RXP2	1230	9000	7770
A61	PCIE_TXN2	1601	9000	7399
A62	PCIE_TXP2	1599	9000	7401
B58	PCIE_RXN3	1251	9000	7749
B59	PCIE_RXP3	1248	9000	7752
A58	PCIE_TXN3	1640	9000	7360
A59	PCIE_TXP3	1639	9000	7361
B55	PCIE_RXN4	1262	9000	7738
B56	PCIE_RXP4	1259	9000	7741
A55	PCIE_TXN4	1588	9000	7412
A56	PCIE_TXP4	1590	9000	7410
B52	PCIE_RXP5	2348	9000	6652
B53	PCIE_RXN5	2348	9000	6652
A52	PCIE_TXP5	1864	9000	7136
A53	PCIE_TXN5	1864	9000	7136

Table 5 PCIE carrier available traces - Device Down

3.1.6 Max trace length and available carrier trace length -

PCIe (Add In Card)

PCIe Add In Card topology

PIN	Name	Module Length	Max Length	Available Carrier length (Device Down Topology)
B68	PCIE_RXP0	1187	7000	5813
B69	PCIE_RXN0	1184	7000	5816
A68	PCIE_TXN0	1639	7000	5361
A69	PCIE_TXP0	1638	7000	5362
B64	PCIE_RXN1	1285	7000	5715
B65	PCIE_RXP1	1285	7000	5715
A64	PCIE_TXN1	1628	7000	5372
A65	PCIE_TXP1	1628	7000	5372
B61	PCIE_RXN2	1229	7000	5771
B62	PCIE_RXP2	1230	7000	5770
A61	PCIE_TXN2	1601	7000	5399
A62	PCIE_TXP2	1599	7000	5401
B58	PCIE_RXN3	1251	7000	5749
B59	PCIE_RXP3	1248	7000	5752
A58	PCIE_TXN3	1640	7000	5360
A59	PCIE_TXP3	1639	7000	5361
B55	PCIE_RXN4	1262	7000	5738
B56	PCIE_RXP4	1259	7000	5741
A55	PCIE_TXN4	1588	7000	5412
A56	PCIE_TXP4	1590	7000	5410
B52	PCIE_RXP5	2348	7000	4652
B53	PCIE_RXN5	2348	7000	4652
A52	PCIE_TXP5	1864	7000	5136
A53	PCIE_TXN5	1864	7000	5136

Table 6 PCIE carrier available traces - Add In Card

3.1.7 Max trace length and available carrier trace length -

PEG (Device Down)

PEG Device Down Topology

PIN	Name	Module Length	Max Length	Available Carrier length (Add In Card Topology)
C52	PEG_RX0+	1023	8000	6977
C53	PEG_RX0-	1023	8000	6977
D52	PEG_TX0+	782	8000	7218
D53	PEG_TX0-	783	8000	7217
C55	PEG_RX1+	1188	8000	6812
C56	PEG_RX1-	1190	8000	6810
D55	PEG_TX1+	1020	8000	6980
D56	PEG_TX1-	1022	8000	6978
C58	PEG_RX2+	1316	8000	6684
C59	PEG_RX2-	1319	8000	6681
D58	PEG_TX2+	1272	8000	6728
D59	PEG_TX2-	1271	8000	6729
C61	PEG_RX3+	1519	8000	6481
C62	PEG_RX3-	1518	8000	6482
D61	PEG_TX3+	1435	8000	6565
D62	PEG_TX3-	1436	8000	6564

Table 7 PEG carrier available traces - Device Down

3.1.8 Max trace length and available carrier trace length -

PEG (Add In Card)

PEG Add In Card In Card Topology

PIN	Name	Module Length	Max Length	Available Carrier length (Add In Card Topology)
C52	PEG_RX0+	1023	8000	6977
C53	PEG_RX0-	1023	8000	6977
D52	PEG_TX0+	782	8000	7218
D53	PEG_TX0-	783	8000	7217
C55	PEG_RX1+	1188	8000	6812
C56	PEG_RX1-	1190	8000	6810
D55	PEG_TX1+	1020	8000	6980

D56	PEG_TX1-	1022	8000	6978
C58	PEG_RX2+	1316	8000	6684
C59	PEG_RX2-	1319	8000	6681
D58	PEG_TX2+	1272	8000	6728
D59	PEG_TX2-	1271	8000	6729
C61	PEG_RX3+	1519	8000	6481
C62	PEG_RX3-	1518	8000	6482
D61	PEG_TX3+	1435	8000	6565
D62	PEG_TX3-	1436	8000	6564

Table 8 PEG carrier available traces - Add In Card

3.2 USB 2.0/3.0

PCOM-B656VGLUSB2.0

Pin#	Pin Name	COMe 3.0 Specification Signals Requiring Module Termination	Pin Typ	B656' Module	PWR Rail / Tolerance (Volt)
A45	USB0-	No termination is required on USB pairs.	I/O USB	PCH TO COM Express Row connector	3.3V Suspend / 3.3V
A46	USB0+				
B45	USB1-				
B46	USB1+				
A42	USB2-				
A43	USB2+				
B42	USB3-				
B43	USB3+				
A39	USB4-				
A40	USB4+				
B39	USB5-				
B40	USB5+				
A36	USB6-				
A37	USB6+				
B36	USB7-				
B37	USB7+				
B44	USB_0_1_OC#	Pulled up to 33V stndby on module with a 10K ohm resister	I CMOS	PU 10K ohm to V3V3A.	3.3V Suspend / 3.3V
A44	USB_2_3_OC#				
B38	USB_4_5_OC#				
A38	USB_6_7_OC#				

Table 9 PCOM-B656VGL USB 2.0

PCOM-B656VGL USB3.0

Pin#	Pin Name	COMe 3.0 Specification Signals Requiring Module Termination	Pin Typ	B656 Module	PWR Rail / Tolerance (Volt)
C3	USB_SSRX0-	AC coupled off Module.	I USB	PCH to COM Express Row connector.	AC coupled off Module.
C4	USB_SSRX0+				
C6	USB_SSRX1-				
C7	USB_SSRX1+				
C9	USB_SSRX2-				
C10	USB_SSRX2+				
C12	USB_SSRX3-				
C13	USB_SSRX3+				
D3	USB_SSTX0-	AC coupled off Module.	O USB	0.1uF AC coupled on Module(Gen3).	AC coupled on Module.
D4	USB_SSTX0+				
D6	USB_SSTX1-				
D7	USB_SSTX1+				
D9	USB_SSTX2-				
D10	USB_SSTX2+				
D12	USB_SSTX3-				
D13	USB_SSTX3+				

Table 10 PCOM-B656VGL USB 3.0

3.2.1 PCB layout guideline - USB2.0/3.0

Parameter	Trace Routing	Trace Routing
Transfer rate / Port	480 Mbit/s	5.0 Gbit/s
Maximum signal line length (coupled traces)	Max. 10.0 inches	Max. 7 inches
Differential Impedance	85 Ω +/-15%	85 Ω +/-15%
Single-ended Impedance	50 Ω +/-15%	50 +/-15%
Trace width (W)	3.5 mil PCB stack-up dependent	3.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	4 mil PCB stack-up dependent	4mil PCB stack-up dependent
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 12mils	Min. 12mils
Spacing between differential pairs	Min. 12mils	Min. 12mils
Length matching between differential pairs (intra-pair)	5 mils	5 mils
Reference plane	GND referenced preferred	GND referenced preferred
Spacing from edge of plane	Min. 10*W mils (W=trace width)	Min. 10*W mils (W=trace width)

Via Usage	Max. 1 vias	Max. 1 vias

Table 11 USB 2.0 / 3.0 Layout information

3.2.2 Reference schematic - PCOM-C605 R2

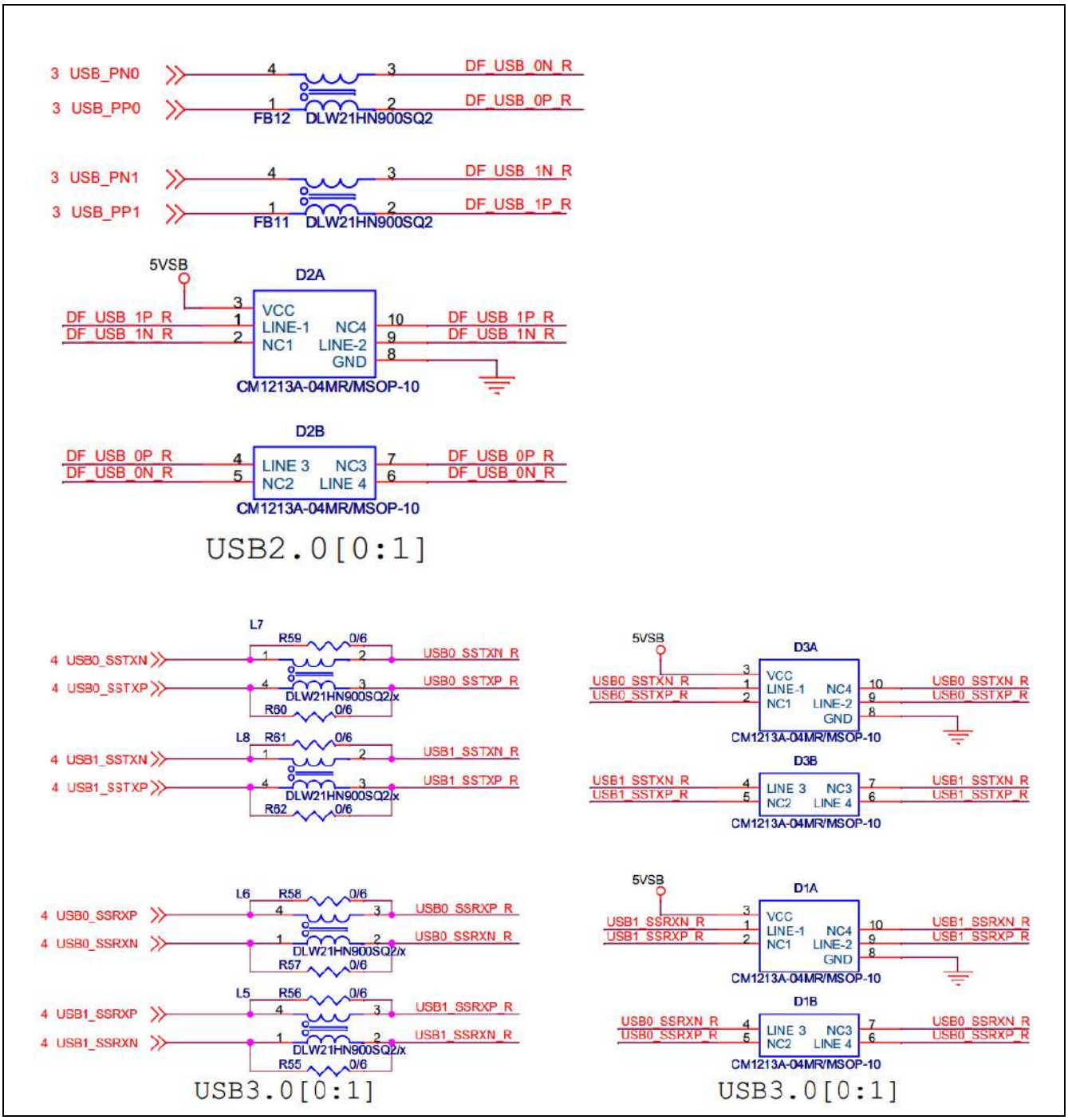


Figure 6 USB 2.0 / 3.0 Reference schematic 1

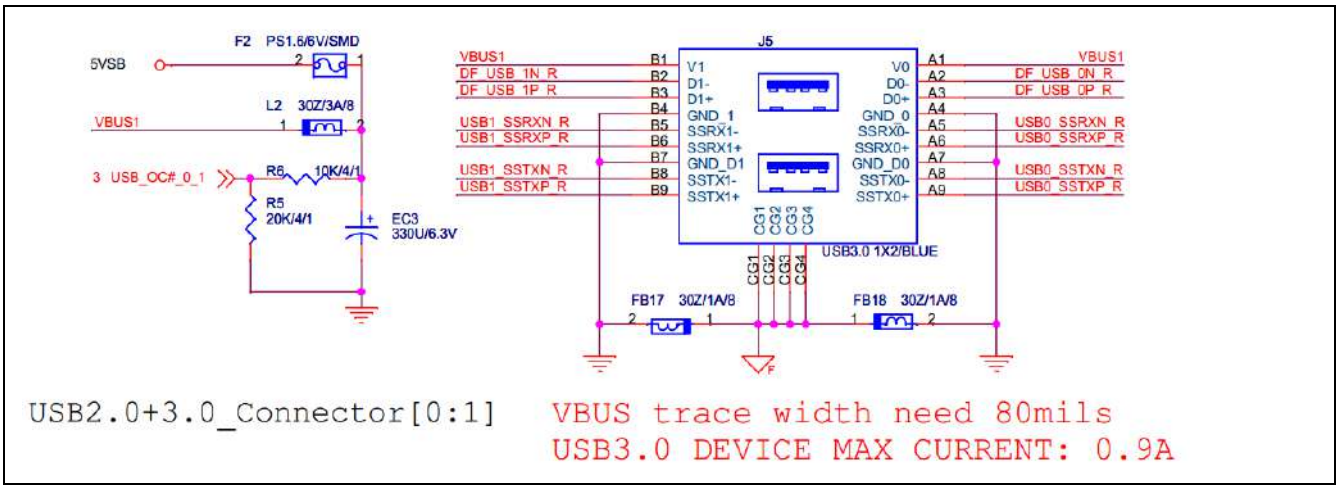


Figure 7 USB 2.0/3.0 Reference schematic 2

3.2.3 Max trace length and available carrier trace length -

USB 2.0 / 3.0

PIN	Name	Module Length	Max Length	Available Carrier length
A45	USB_PN0	1966	10000	8034
A46	USB_PP0	1965	10000	8035
B45	USB_PN1	2001	10000	7999
B46	USB_PP1	2001	10000	7999
A42	USB_PN2	2216	10000	7784
A43	USB_PP2	2216	10000	7784
B42	USB_PN3	2069	10000	7931
B43	USB_PP3	2071	10000	7929
A39	USB_PN4	2555	10000	7445
A40	USB_PP4	2557	10000	7443
B39	USB_PN5	1826	10000	8174
B40	USB_PP5	1825	10000	8175
A36	USB_PN6	2727	10000	7273
A37	USB_PP6	2731	10000	7269
B36	USB_PN7	1664	10000	8336
B37	USB_PP7	1667	10000	8333
D4	USB_SSTX0+	2844	7000	4156
D3	USB_SSTX0-	2843	7000	4157
D7	USB_SSTX1+	2606	7000	4394
D6	USB_SSTX1-	2605	7000	4395

D10	USB_SSTX2+	2674	7000	4326
D9	USB_SSTX2-	2678	7000	4322
D13	USB_SSTX3+	2324	7000	4676
D12	USB_SSTX3-	2325	7000	4675
C4	USB_SSRX0+	2915	7000	4085
C3	USB_SSRX0-	2914	7000	4086
C7	USB_SSRX1+	2748	7000	4252
C6	USB_SSRX1-	2746	7000	4254
C10	USB_SSRX2+	2258	7000	4742
C9	USB_SSRX2-	2258	7000	4742
C13	USB_SSRX3+	2366	7000	4634
C12	USB_SSRX3-	2361	7000	4639

Table 12 Carrier available traces - USB 2.0 / 3.0

3.3 DDI

PCOM-B656VGL DDI1

Pin#	Pin Name	COMe 3.0 Specification Signals Requiring Module Termination	Pin Typ	B656 Module	PWR Rail / Tolerance (Volt)
D26	DDI1_PAIR0+	AC coupled off Module	O DDI	AC coupled off Module	AC coupled off Module
D27	DDI1_PAIR0-				
D29	DDI1_PAIR1+				
D30	DDI1_PAIR1-				
D32	DDI1_PAIR2+				
D33	DDI1_PAIR2-				
D36	DDI1_PAIR3+				
D37	DDI1_PAIR3-				
D15	DDI1_CTRLCLK_AUX+		I/O DDI		AC coupled on Module
			I/O OD CMOS		3.3V / 3.3V
D16	DDI1_CTRLDATA_AUX-		I/O DDI		AC coupled on Module
			I/O OD CMOS		3.3V / 3.3V
D34	DDI1_DDC_AUX_SEL	1M pull-down to logic ground on the module	I CMOS	1M pull-down to GND on the Module	3.3V / 3.3V
C24	DDI1_HPD		I CMOS	Follow INTEL WHL PDG : PD 100K ohm to GND	3.3V / 3.3V

Table 13 PCOM-B656VGLDDI1

PCOM-B656VGL DDI2

Pin#	Pin Name	COMe 3.0 Specification Signals Requiring Module Termination	Pin Typ	B656 Module	PWR Rail / Tolerance (Volt)
D39	DDI2_PAIR0+	AC coupled off Module	O DDI	AC coupled off Module	AC coupled off Module
D40	DDI2_PAIR0-				
D42	DDI2_PAIR1+				
D43	DDI2_PAIR1-				
D46	DDI2_PAIR2+				
D47	DDI2_PAIR2-				
D49	DDI2_PAIR3+				
D50	DDI2_PAIR3-				
C32	DDI2_CTRLCLK_AUX+		I/O DDI	1. Module follow COM Express Spec Figure 4-1 : Dual-Mode COM Express Module Implementation	AC coupled on Module
			I/O OD CMOS		3.3V / 3.3V
C33	DDI2_CTRLDATA_AUX-		I/O DDI		AC coupled on Module
			I/O OD CMOS		3.3V / 3.3V
C34	DDI2_DDC_AUX_SEL	1M pull-down to logic ground on the module	I CMOS	1M pull-down to GND on the Module	3.3V / 3.3V
D44	DDI2_HPD		I CMOS	Follow INTEL WHL PDG : PD 100K ohm to GND	3.3V / 3.3V

Table 14 PCOM-B656VGL DDI2

3.3.1 PCB layout guideline - DDI (DP)

Parameter	Trace Routing
Transfer Rate	Max. 5.4 Gbit/s
Maximum signal line length (coupled traces)	4.1 inches
Differential Impedance	85 Ω +/-15%
Single-ended Impedance	50 Ω +/-15%
Trace width (W)	3.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	4mil PCB stack-up dependent
Spacing between pairs-to-pair	Min. 12mils
Spacing between differential pairs and high-speed periodic signals	Min. 15mils
Spacing between differential pairs and low-speed non periodic signals	Min. 15mils
Length matching between differential pairs (intra-pair)	Max. 5 mils
Spacing from edge of plane	Min. 10*W mils (W=trace width)
Via Usage	Max. 1
AC coupling capacitors	100nF

Table 18 DDI Layout information

3.3.2 Reference schematic - PCOM-C605 R2

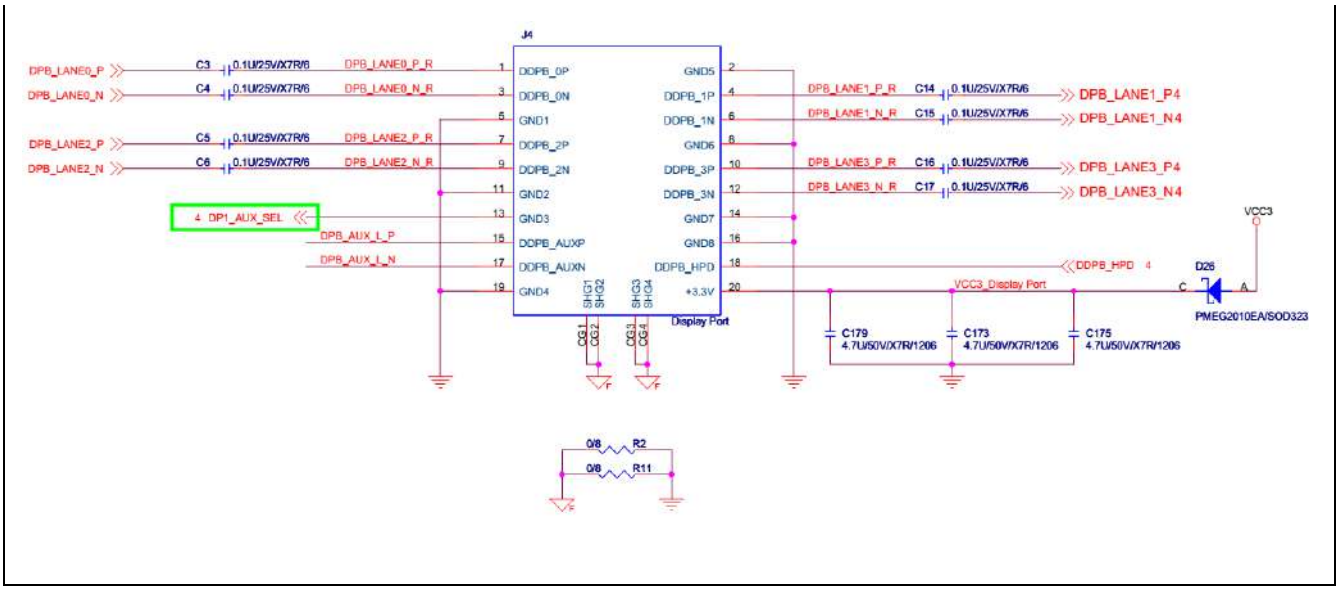


Figure 8 Reference schematic - DDI

3.3.3 Max trace length and available carrier trace length - DDI

PIN	Name	Module Length	Max Length	Available Carrier length
D26	DDI1_PAIR0+	691	7000	6309
D27	DDI1_PAIR0-	691	7000	6309
D29	DDI1_PAIR1+	895	7000	6105
D30	DDI1_PAIR1-	897	7000	6103
D32	DDI1_PAIR2+	741	7000	6259
D33	DDI1_PAIR2-	741	7000	6259
D36	DDI1_PAIR3+	599	7000	6401
D37	DDI1_PAIR3-	600	7000	6400
D39	DDI2_PAIR0+	878	7000	6122
D40	DDI2_PAIR0-	878	7000	6122
D42	DDI2_PAIR1+	695	7000	6305
D43	DDI2_PAIR1-	695	7000	6305
D46	DDI2_PAIR2+	762	7000	6238
D47	DDI2_PAIR2-	762	7000	6238
D49	DDI2_PAIR3+	646	7000	6354
D50	DDI2_PAIR3-	647	7000	6353

Table 19 Carrier available traces - DDI

3.4 LAN

PCOM-B656VGL LAN

Pin#	Pin Name	COMe 3.0 Specification Signals Requiring Module Termination	Pin Typ	B656 Module	PWR Rail / Tolerance (Volt)
A12	GBE0_MDI0-	-	I/O Analog	Media Dependent Interface signal , I219 phy chip on module	3.3V max Suspend
A13	GBE0_MDI0+	-			
A9	GBE0_MDI1-	-			
A10	GBE0_MDI1+	-			
A6	GBE0_MDI2-	-			
A7	GBE0_MDI2+	-			
A2	GBE0_MDI3-	-			
A3	GBE0_MDI3+	-			
A8	GBE0_LINK#	-	OD CMOS	Gigabit Ethernet Controller 0 link indicator, active low.	3.3V Suspend / 3.3V
A4	GBE0_LINK100#	-	OD(I/O) CMOS	Indicate Gbe signal speed.	3.3V Suspend / 3.3V
A5	GBE0_LINK1000#	-	OD(I/O) CMOS	Indicate Gbe signal speed.	3.3V Suspend / 3.3V
A14	GBE0_CTREF	-	REF	Reserved resistor (NP) (I219) internal 0.9V to central Volt)	GND min 3.3V max
B2	GBE0_ACT#	-	OD(I/O) CMOS	I219 PHY chip to COM Express Row connector	3.3V Suspend / 3.3V

Table 20 PCOM-B656VGLLAN

3.4.1 PCB layout guideline - LAN

Parameter	Trace Routing
Differential Impedance	100 Ω +/-10%
Single-ended Impedance	50 Ω +/-10%
Trace width (W)	4 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	9 mil PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Min. 28 mils
Length matching between RX and TX pairs (inter-pair)	Max. 10mils
Spacing from edge of plane	Min. 10*W mils (W=trace width)

Table 151 LAN Layout information

3.4.2 Reference schematic - PCOM-C605 R2

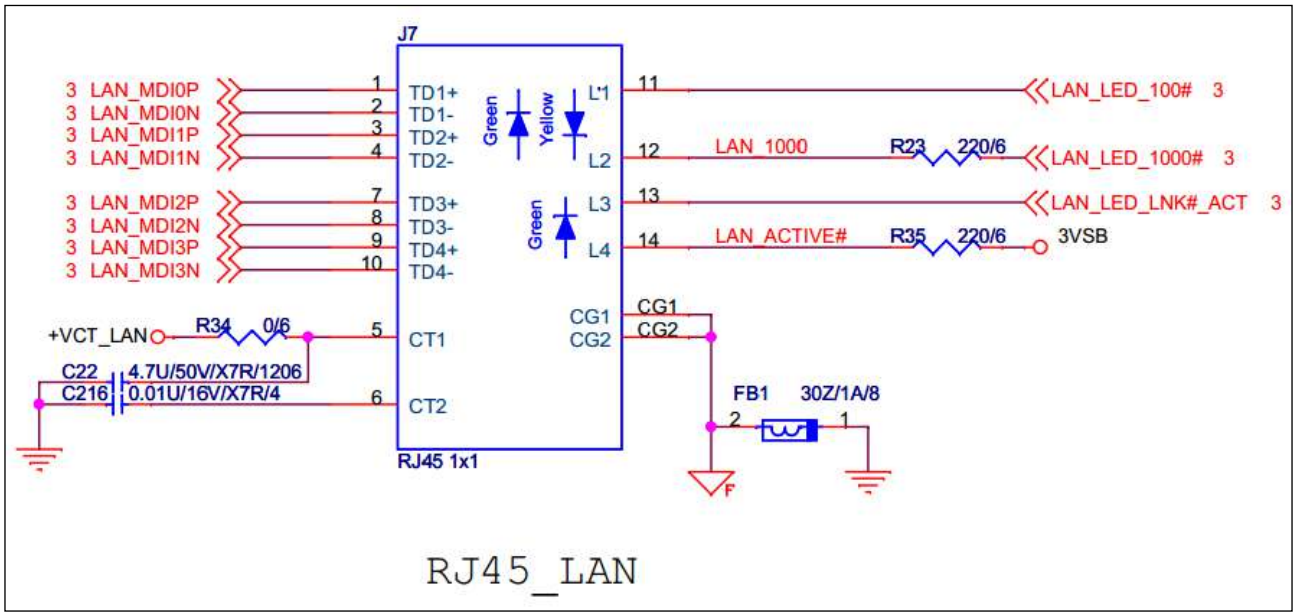


Figure 9 Reference schematic - LAN

3.4.3 Max trace length and available carrier trace length - LAN

PIN	Name	Module Length	Max Length	Available Carrier length
A13	GBE0_MDI0+	824	4000	3176
A12	GBE0_MDI0-	827	4000	3173
A10	GBE0_MDI1+	827	4000	3173
A9	GBE0_MDI1-	828	4000	3172
A7	GBE0_MDI2+	827	4000	3173
A6	GBE0_MDI2-	827	4000	3173
A3	GBE0_MDI3+	837	4000	3163
A2	GBE0_MDI3-	835	4000	3165

Table 22 Carrier available traces - LAN

3.5 SATA

PCOM-B656VGL SATA

Pin#	Pin Name	COMe 3.0 Specification Signals Requiring Module Termination	Pin Typ	B656 Module	PWR Rail / Tolerance (Volt)
A16	SATA0_TX+	AC coupled on the Module	O SATA	0.01uF AC coupled on the Module(Gen3)	AC coupled off Module
A17	SATA0_TX-				
A19	SATA0_RX+		I SATA		
A20	SATA0_RX-				
A22	SATA2_TX+		O SATA		
A23	SATA2_TX-				
A25	SATA2_RX+		I SATA		
A26	SATA2_RX-				
B16	SATA1_TX+		O SATA		
B17	SATA1_TX-				
B19	SATA1_RX+		I SATA		
B20	SATA1_RX-				
B22	SATA3_TX+		O SATA		
B23	SATA3_TX-				
B25	SATA3_RX+		I SATA		
B26	SATA3_RX-				
A28	SATA_ACT#		O/D(I/O) CMOS	PU 10K ohm to V3P3S	3.3V / 3.3V
B18	SUS_SATA#	Indicates imminent suspend operation ; used to notify LPC devices.	O CMOS	PCH to COM Express Row connector	3.3v Suspend / 3.3V

Table 163 PCOM-B656VGL SATA

3.5.1 PCB layout guideline -SATA

Parameter	Trace Routing
Transfer Rate	Up to 6.0 Gbit/s
Maximum signal line length (coupled traces)	7.0 inches
Differential Impedance	85 Ω +/-15%
Single-ended Impedance	50 Ω +/-15%
Trace width (W)	3.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	4mil PCB stack-up dependent
Spacing between differential pairs and high-speed periodic signals	Min. 15 mils
Spacing between differential pairs and low-speed non periodic signals	Min. 15 mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Spacing from edge of plane	Min. 10*W mils

	(W=trace width)
Via Usage	A maximum of 1 vias is recommended.
AC Coupling capacitors	10nF

Table 24 SATA layout information

3.5.2 Reference schematic - PCOM-C605 R2

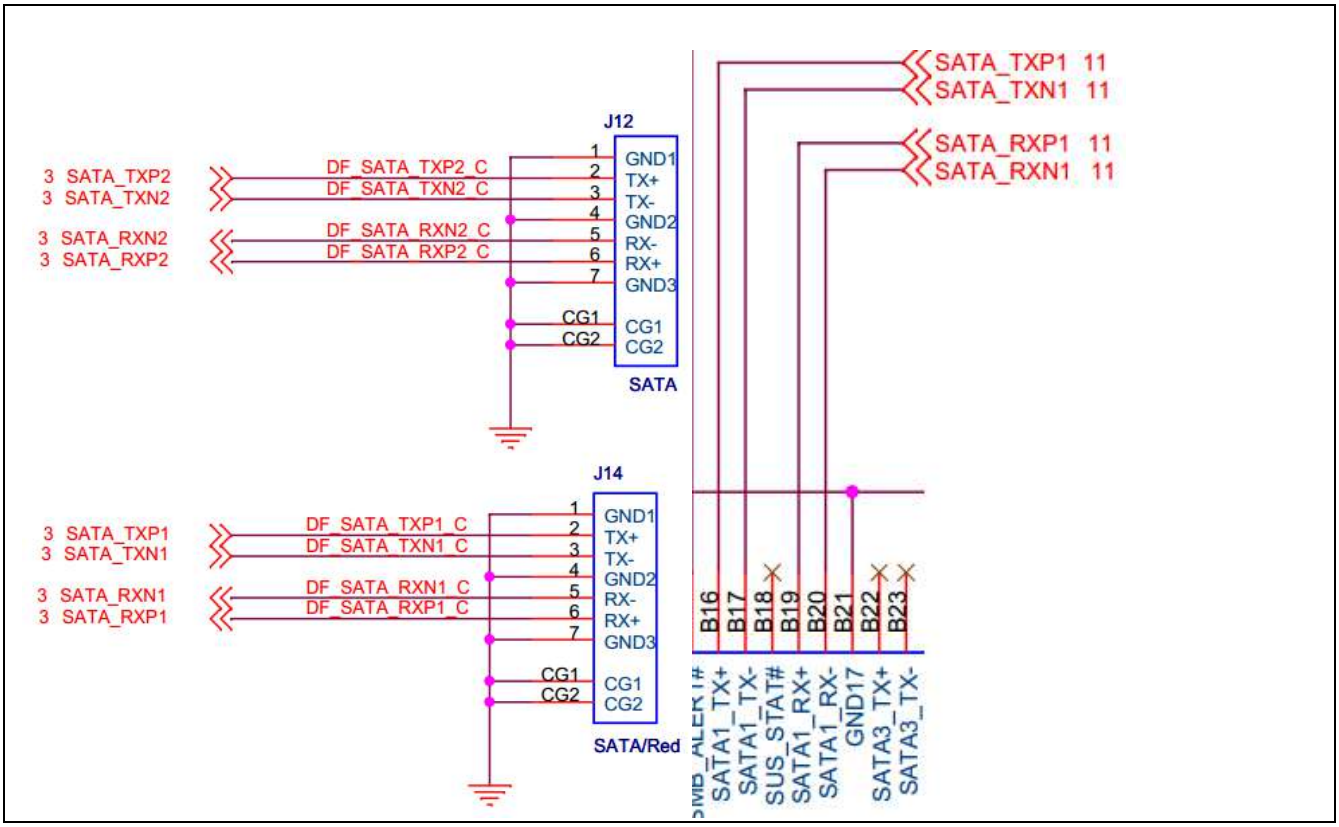


Figure 10 Reference schematic - SATA

3.5.3 Max trace length and available carrier trace length -

SATA

Name	Module Length	Max Length	Available Carrier length	Name
SATA0_RX+	1998	7000	5002	SATA0_RX+
SATA0_RX-	1995	7000	5005	SATA0_RX-
SATA0_TX+	1989	7000	5011	SATA0_TX+
SATA0_TX-	1988	7000	5012	SATA0_TX-

SATA1_RX+	1831	7000	5169	SATA1_RX+
SATA1_RX-	1828	7000	5172	SATA1_RX-
SATA1_TX+	1675	7000	5325	SATA1_TX+
SATA1_TX-	1679	7000	5321	SATA1_TX-

Table 25 Carrier available traces - SATA

3.6 LVDS

PCOM-B656VGL LVDS

Pin#	Pin Name	COMe 3.0 Specification (Signals Requiring Module Termination)	Pin Typ	B656 Module	PWR Rail / Tolerance (Volt)
A71	LVDS_A0+	-	O LVDS	According to COMe spec 3.0 table 4.37 lvds/eDP pin assignment definition co-lay,default module TPN3460 to LVDS COMe Row connector	LVDS
A72	LVDS_A0-	-			
A73	LVDS_A1+	-			
A74	LVDS_A1-	-			
A75	LVDS_A2+	-			
A76	LVDS_A2-	-			
A78	LVDS_A3+	-			
A79	LVDS_A3-	-			
A81	LVDS_A_CK+	-			
A82	LVDS_A_CK-	-			
B71	LVDS_B0+	-			
B72	LVDS_B0-	-			
B73	LVDS_B1+	-			
B74	LVDS_B1-	-			
B75	LVDS_B2+	-			
B76	LVDS_B2-	-			
B77	LVDS_B3+	-			
B78	LVDS_B3-	-			
B81	LVDS_B_CK+	-			
B82	LVDS_B_CK-	-			
B83	LVDS_BKLT_CTRL	-	O CMOS	LVDS_BKLT_CTRL	3.3V/3.3V
A77	LVDS_VDD_EN	-		LVDS pannel power enable	
B79	LVDS_BKLT_EN	-		According to COMe spec 3.0 table 4.37 lvds/eDP pin assignment definition co-lay,default module TPN3460 to LVDS COMe Row connector	
A83	LVDS_I2C_CK	-			
A84	LVDS_I2C_DAT	-	OD(I/O) CMOS		

Table 26 PCOM-B656VGL LVDS

3.6.1 PCB layout guideline - LVDS

Parameter	Trace Routing
Maximum signal line length to the LVDS connector (coupled traces)	10 inches
Differential Impedance	85 Ω +/-15%
Single-ended Impedance	50 Ω +/-15%
Trace width (W)	PCB stack-up dependent
Spacing between differential pair signals (intra-pair) (S)	30 PCB stack-up dependent

Table 17 LVDS Layout information

3.6.2 Reference schematic - PCOM-C605 R2

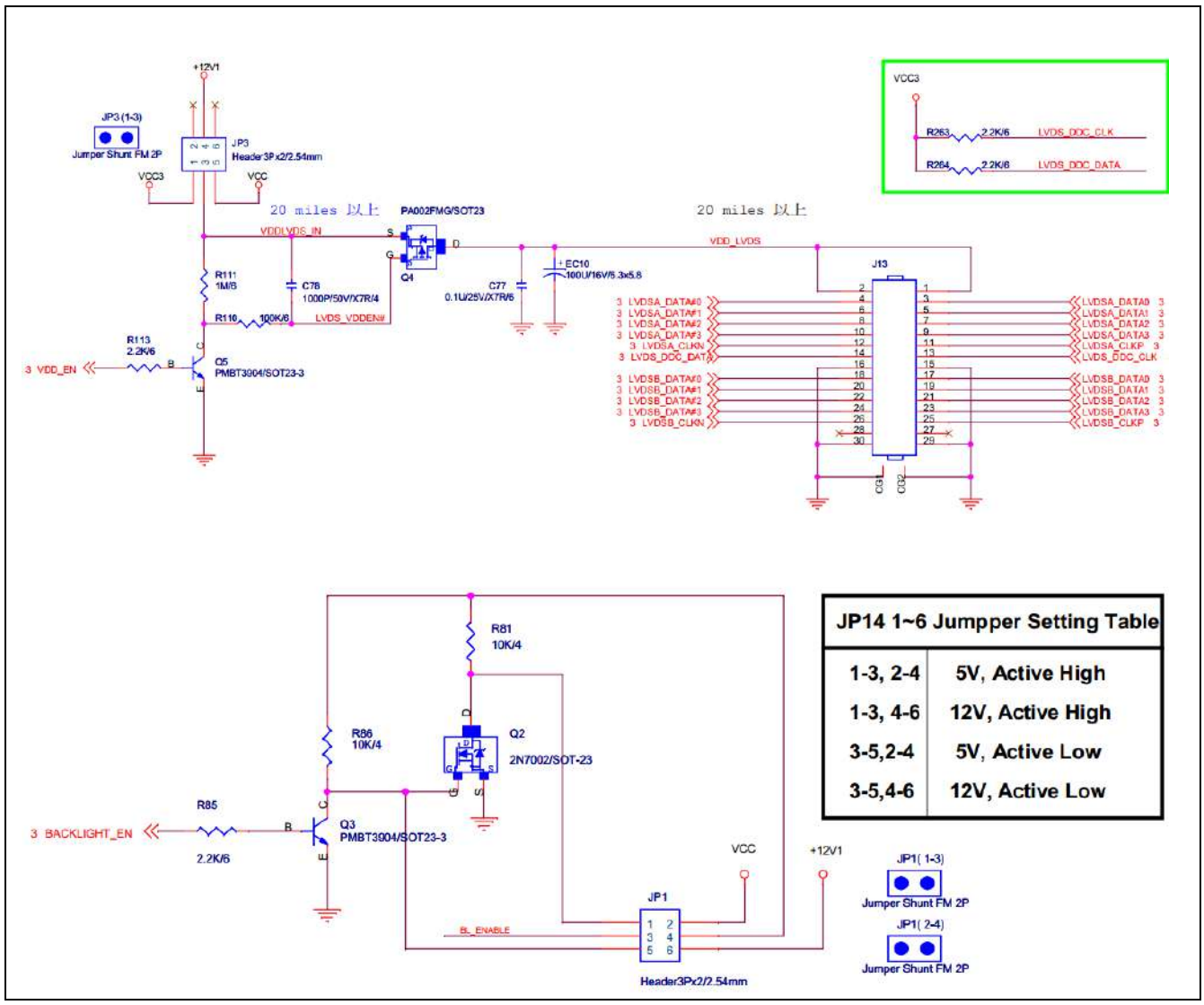


Figure 11 Reference schematic - LVDS

3.6.3 Max trace length and available carrier trace length - LVDS

PIN	Name	Module Length	Max Length	Available Carrier length
A71	LVDS_A0+	1555	10000	8445
A72	LVDS_A0-	1557	10000	8443
A73	LVDS_A1+	1476	10000	8524
A74	LVDS_A1-	1475	10000	8525
A75	LVDS_A2+	1486	10000	8514
A76	LVDS_A2-	1486	10000	8514
A78	LVDS_A3+	1470	10000	8530
A79	LVDS_A3-	1470	10000	8530

A81	LVDS_A_CK+	1239	10000	8761
A82	LVDS_A_CK-	1235	10000	8765
A83	LVDS_I2CCLK	729	12000	11271
A84	LVDS_I2CDAT	729	12000	11271

Table 28 Carrier available traces – LVDS Channel A

B71	LVDS_B0+	1628	10000	8372
B72	LVDS_B0-	1628	10000	8372
B73	LVDS_B1+	1570	10000	8430
B74	LVDS_B1-	1570	10000	8430
B75	LVDS_B2+	1686	10000	8314
B76	LVDS_B2-	1686	10000	8314
B77	LVDS_B3+	1667	10000	8333
B78	LVDS_B3-	1667	10000	8333
B81	LVDS_B_CK+	1433	10000	8567
B82	LVDS_B_CK-	1430	10000	8570
B71	LVDS_B0+	1628	10000	8372

Table 29 Carrier available traces – LVDS Channel B

3.7 UART

PCOM-B656VGL UART

Pin#	Pin Name	COMe 3.0 Specification Signals Requiring Module Termination	Pin Typ	B656 Module	PWR Rail / Tolerance (Volt)
A98	SER0_TX	Re-claimed from pins that are VCC_12V supply pins.	O CMOS	Series connection Schottky diode and level shift	5V/12V
A99	SER0_RX		I CMOS		
A101	SER1_TX		O CMOS		
A102	SER1_RX		I CMOS		

Table 30 PCOM-B656VGL UART

3.7.1 Reference schematic - PCOM-C605 R2

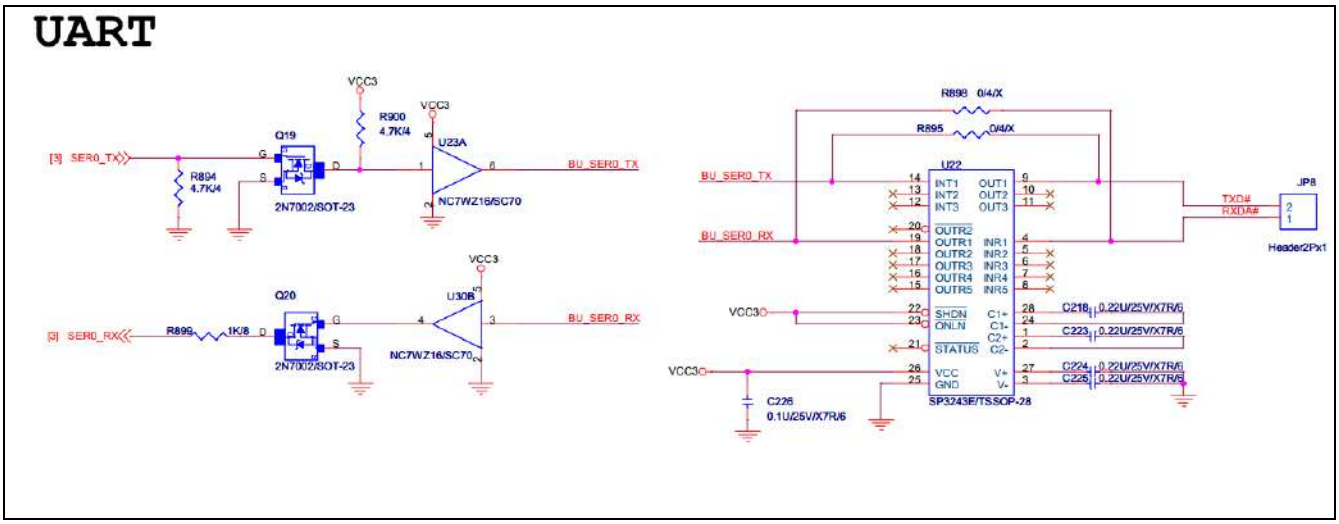


Figure 12 Reference schematic - UART

3.8 I2C

PCOM-B656VGL I2C

Pin#	Pin Name	COMe 3.0 Specification (Signals Requiring Module Termination)	Pin Typ	B656 Module	PWR Rail / Tolerance (Volt)
B33	I2C_CK	Pulled-up to 3.3V standby on module with a 2.2K ohm resistor	I/O OD CMOS	PU 1K ohm to V3P3A	3.3V Suspend
B34	I2C_DAT				

Table 31 PCOM-B656VGL I2C

3.9 SMBus

PCOM-B656VGL SMBus

Pin#	Pin Name	COMe 3.0 Specification (Signals Requiring Module	Pin Typ	B656 Module	PWR Rail / Tolerance (Volt)
B13	SMB_CK	Pulled-up to 3.3V standby on module with a 2.2K ohm resistor	I/O OD CMOS	PU 2.2K ohm to V3P3A	3.3V Suspend / 3.3V
B14	SMB_DAT				
B15	SMB_ALERT#	-	I CMOS	PU 8.2K ohm to V3P3A	

Table 32 PCOM-B656VGL SMBus

3.9 GPIO

PCOM-B656VGL GPIO

Pin#	Pin Name	COMe 3.0 Specification Signals Requiring Module Termination	Pin Typ	B656 Module	PWR Rail / Tolerance (Volt)
A54	GPI0	Pulled high internally on the module	I CMOS	PU 4.7K ohm to V3P3S.	3.3V/3.3V
A63	GPI1				
A67	GPI2				
A85	GPI3				
A93	GPO0	-	O CMOS	EC to COM Express Row connector	3.3V/3.3V
B54	GPO1	-			
B57	GPO2	-			
B63	GPO3	-			

Table 33 PCOM-B656VGL GPIO

3.10 LPC

PCOM-B656VGL LPC

Pin#	Pin Name	COMe 3.0 Specification Signals Requiring Module Termination	Pin Typ	B656 Module	PWR Rail / Tolerance (Volt)
A50	LPC_SERIRQ	Pulled-up to 3.3V on module with a 8.2K resistor	I/O CMOS	PCH PU 10K ohm to V3P3S.	3.3V/3.3V
B3	LPC_FRAME#		O CMOS	PCH to COMe Row connector	
B4	LPC_AD0	-	I/O CMOS		
B5	LPC_AD1	-			
B63	LPC_AD2	-			
B7	LPC_AD3	-			
B8	LPC_DRQ0#	-	I CMOS	NC	
B9	LPC_DRQ1#	-		Series connection 22 ohm	
B10	LPC_CLK	-	O CMOS		

Table 34 PCOM-B656VGL LPC

3.10.1 PCB layout guideline - LPC

Parameter	Trace Routing
Transfer Rate	25/33 MHz
Maximum signal line length (coupled traces)	Max. 10 inches
Single-ended Impedance	50 +/-15%
Trace Width	3.5 mil PCB stack-up dependent
Trace Spacing	4mil

	PCB stack-up dependent

Table 35 LPC Layout information

3.10.2 Reference schematic - PCOM-C605 R2

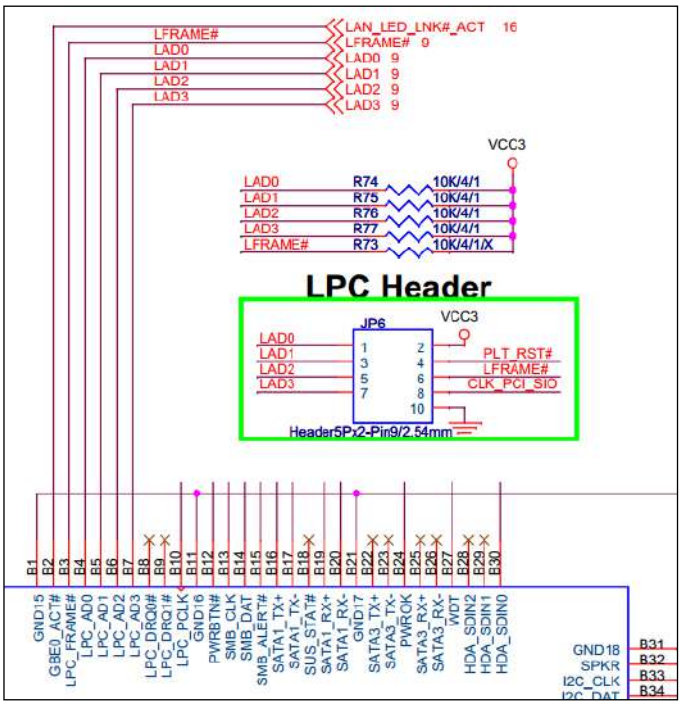


Figure 13 Reference schematic - LPC

3.11 SPI

An external SPI BIOS is designed on the Carrier board, which allows the Module boot from the Carrier SPI BIOS. To achieve this function, the BIOS_DIS0# and BIOS_DIS1# must be designed as a selectable method on the Carrier.

PCOM-B656VGL SPI

Pin#	Pin Name	COMe 3.0 Specification Signals Requiring Module Termination	Pin Typ	B656 Module	PWR Rail / Tolerance (Volt)
A34	BIOS_DIS0#	Pulled-up to 3.3V on module with a 10K ohm resistor	I CMOS	PU 10K ohm to V3P3A.	NA
B88	BIOS_DIS1#				
A91	SPI_POWER	Power supply for carrier board SPI - sourced from Module - nominally 3.3V The module shall provide a minimum of 100 mA on SPI_POWER	O	SPI_POWER	3.3V Suspend / 3.3V
A92	SPI_MISO	All such terminations shallbe on the Module When supporting carrier board based SPI devices ,the SPI MISO line shall have a series resistor of 33 ohm	I CMOS	1. PU 3.3K ohm to SPI_POWER 2. 33 ohm series connector (Accrding to Intel Platform Design Guide)	
A94	SPI_CLK	All such terminations shallbe on the Module	O CMOS	33 ohm series connection (According to Intel Platform Design Guide)	
A95	SPI_MOSI				
B97	SPI_CS#	-	O CMOS	-	

Table 36 PCOM-B656VGL SPI

3.11.1 Reference schematic - PCOM-C605 R2

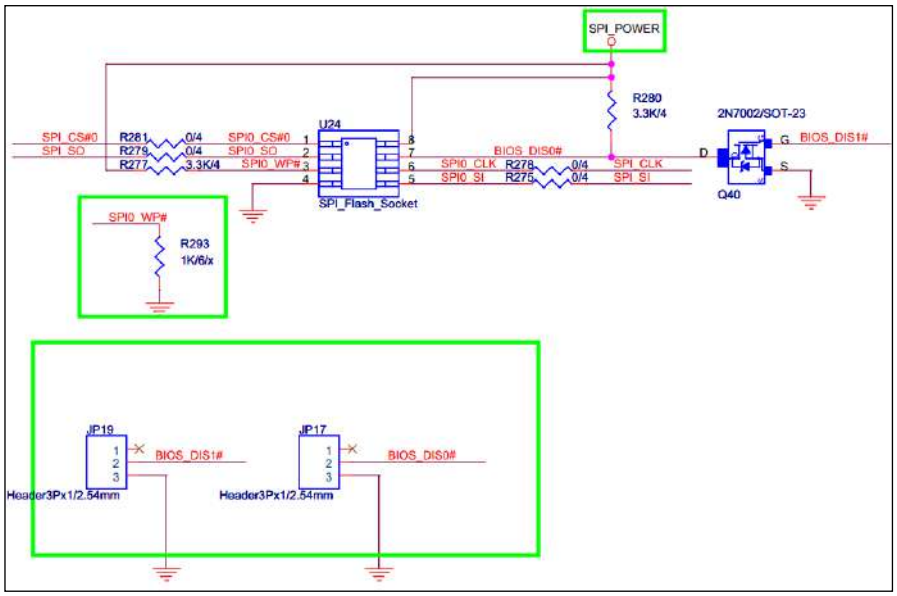


Figure 14 Reference schematic - SPI

4 Power

PCOM-B656VGL is designed for both AT and ATX power mode, which depends on the power mode design on carrier board. The following ATX and AT mode power sequences are provided for the carrier design guideline.

4.1 Power sequence

The ATX power sequence is based on PCOM-B656VGL-R0 with evaluation carrier PCOM-C605-R2.

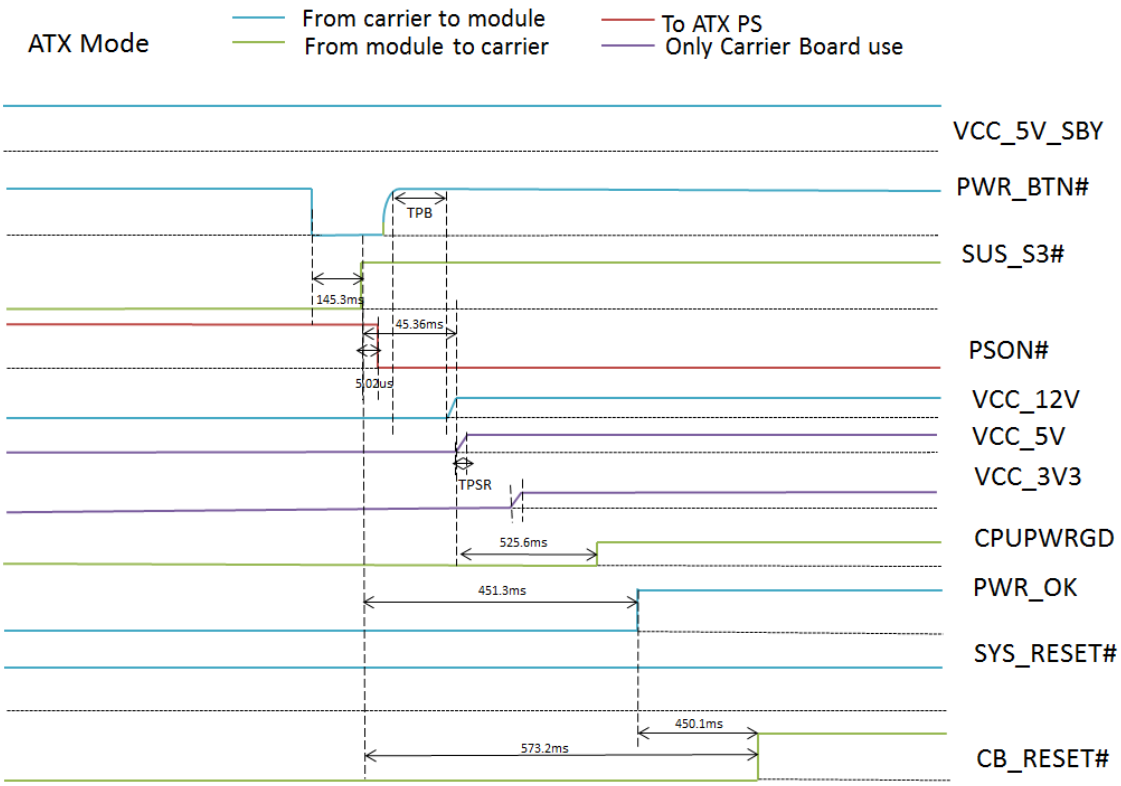


Figure 15 PCOM-B656VGL ATX Mode power sequence

The AT power sequence is based on PCOM-B656VGL-R0 with evaluation carrier PCOM-C605-R2.

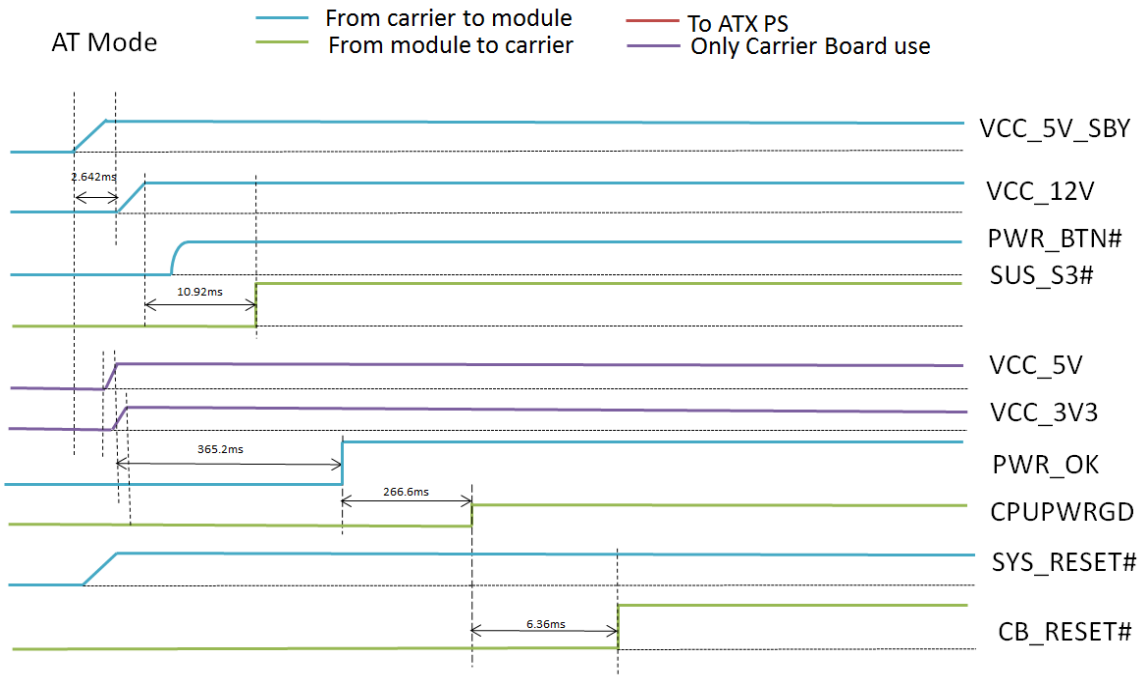


Figure 16 PCOM-B656VGL AT Mode power sequence

5 Mechanical

5.1 PCOM-B656VGL Dimension

PCOM-B656VGL top side view dimension

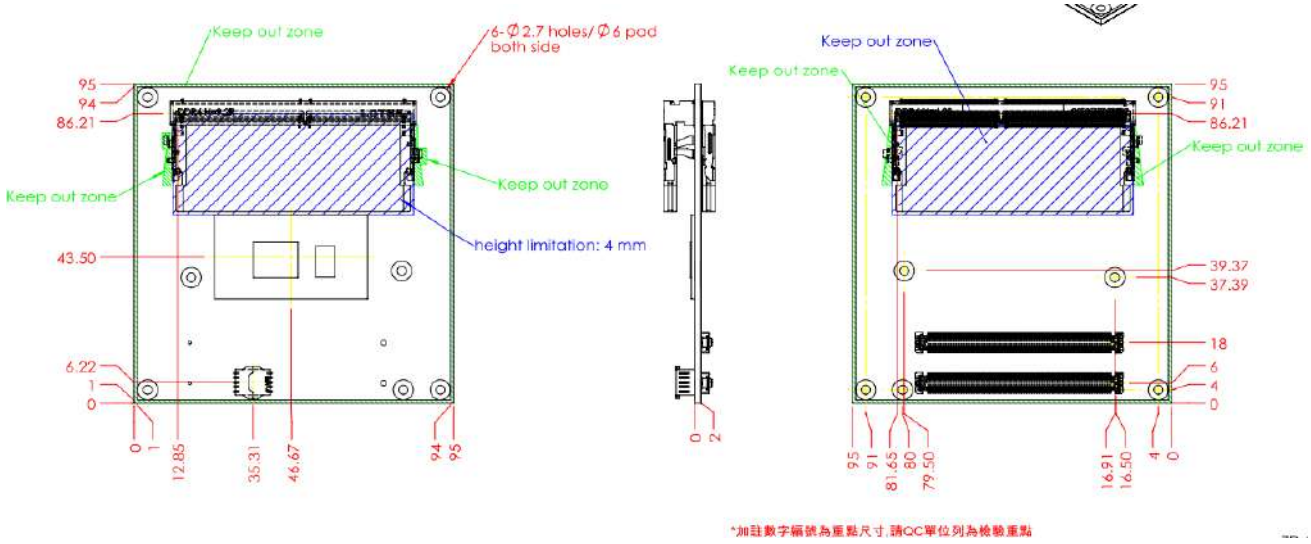


Figure 17 PCOM-B656VGL Dimension – TOP & Bottom

PCOM-B656VGL side view dimension, along with a heat sink / cooler.

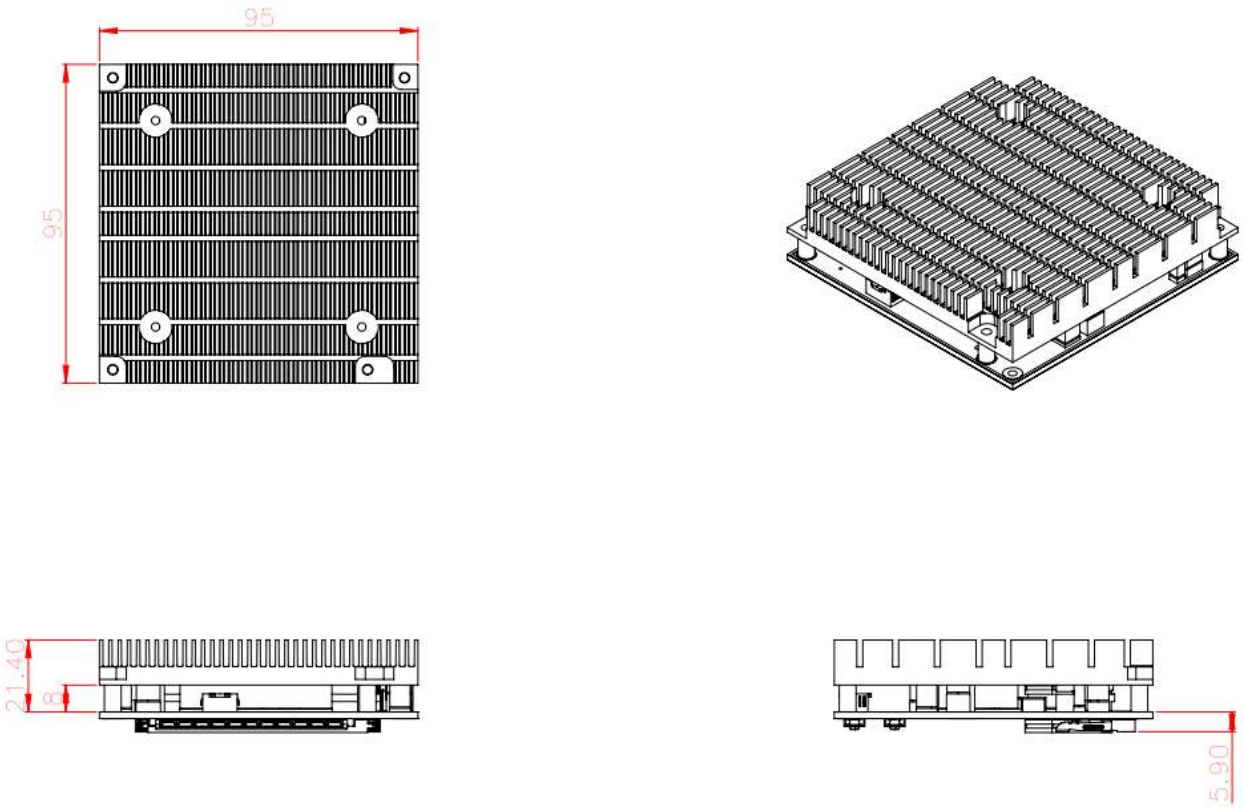
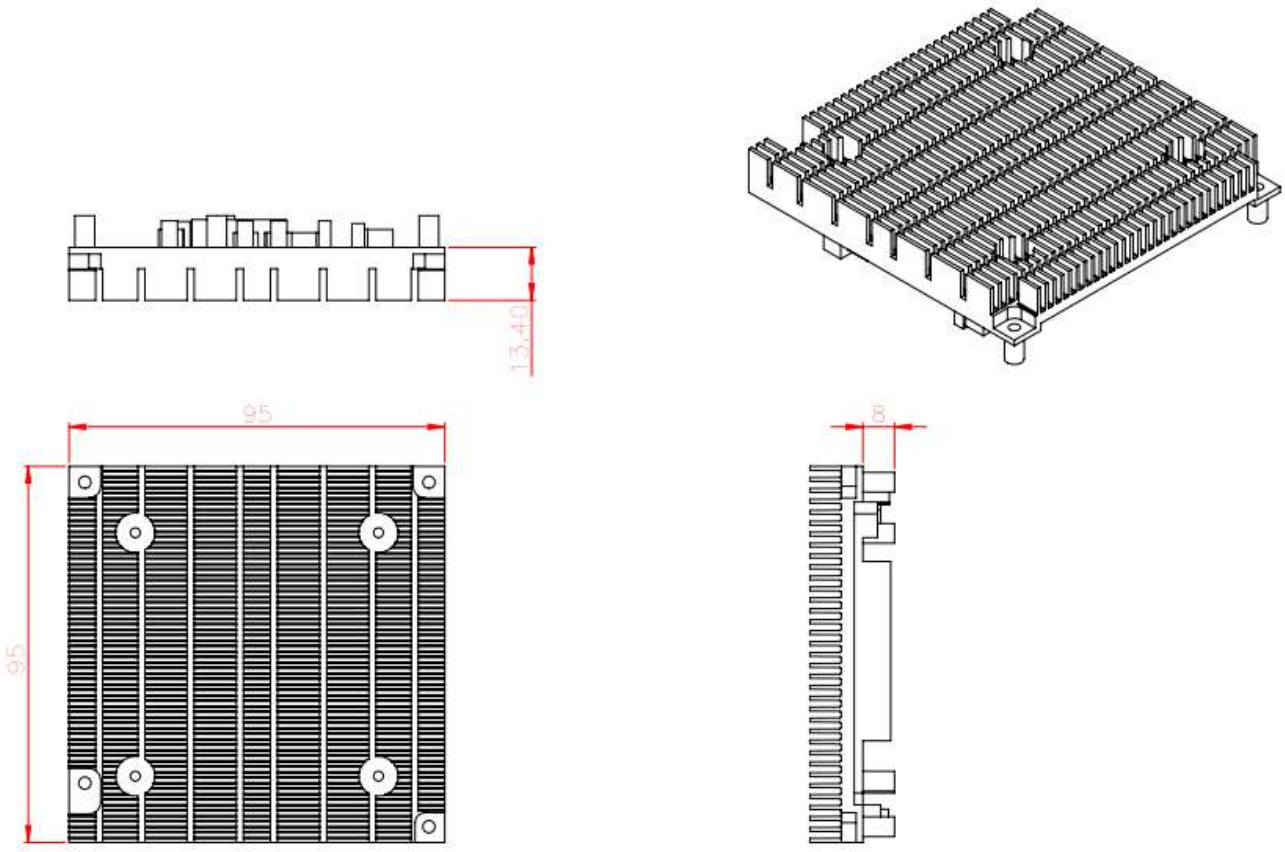


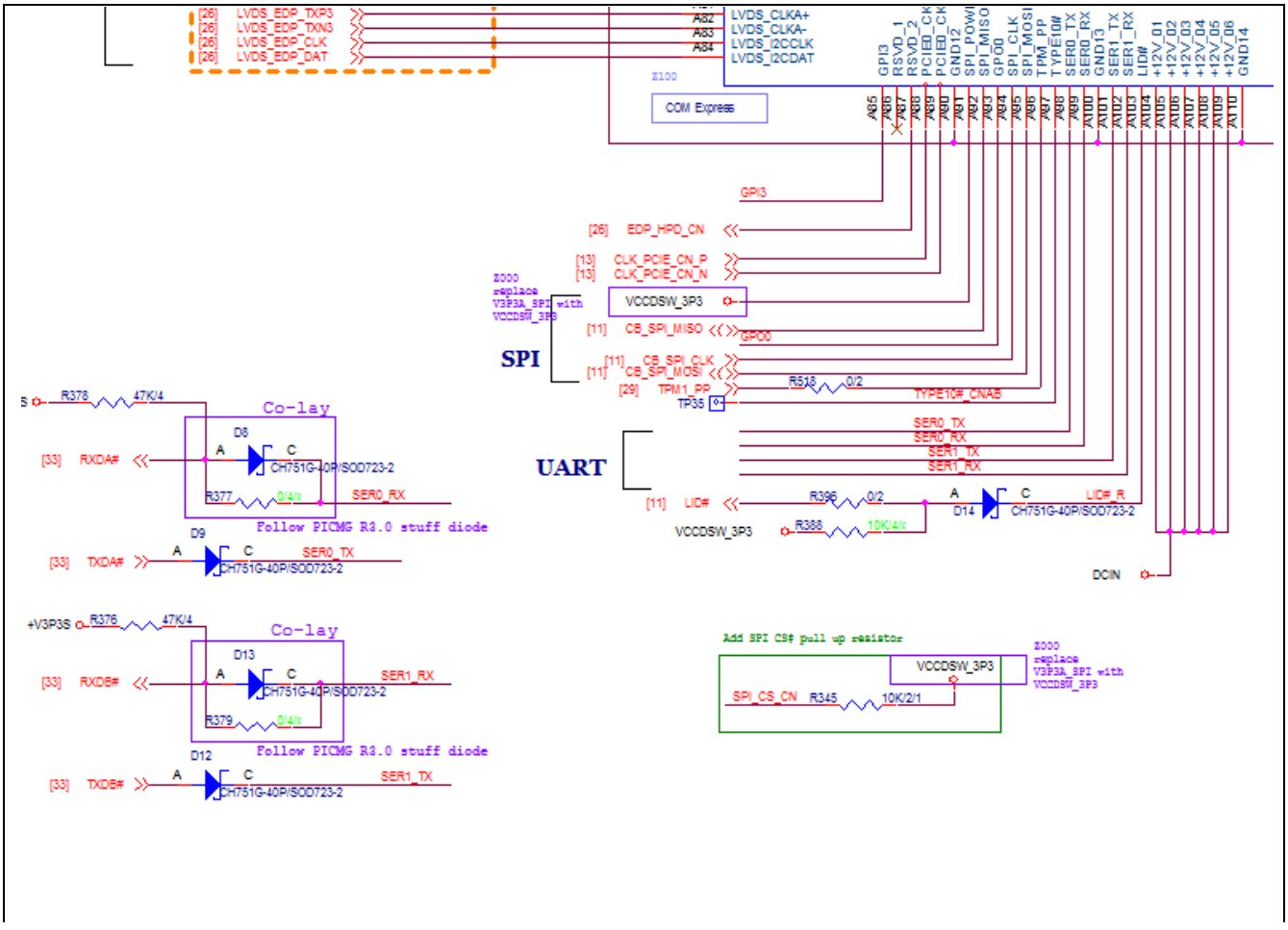
Figure 18 PCOM-B656VGLDimension - Side view



6 COM Express Module and Carrier Protection design

6.1 Module protection

PCOM-B656VGL Type 6 is also compatible with COM Express Type 2 carrier, Schottky diode protection has been design on the COM Express module for Serial Port, FAN(PWMOUT & TACHIN), LID and SLEEP. Please refer to Fig.20 Module circuit protection schematic.



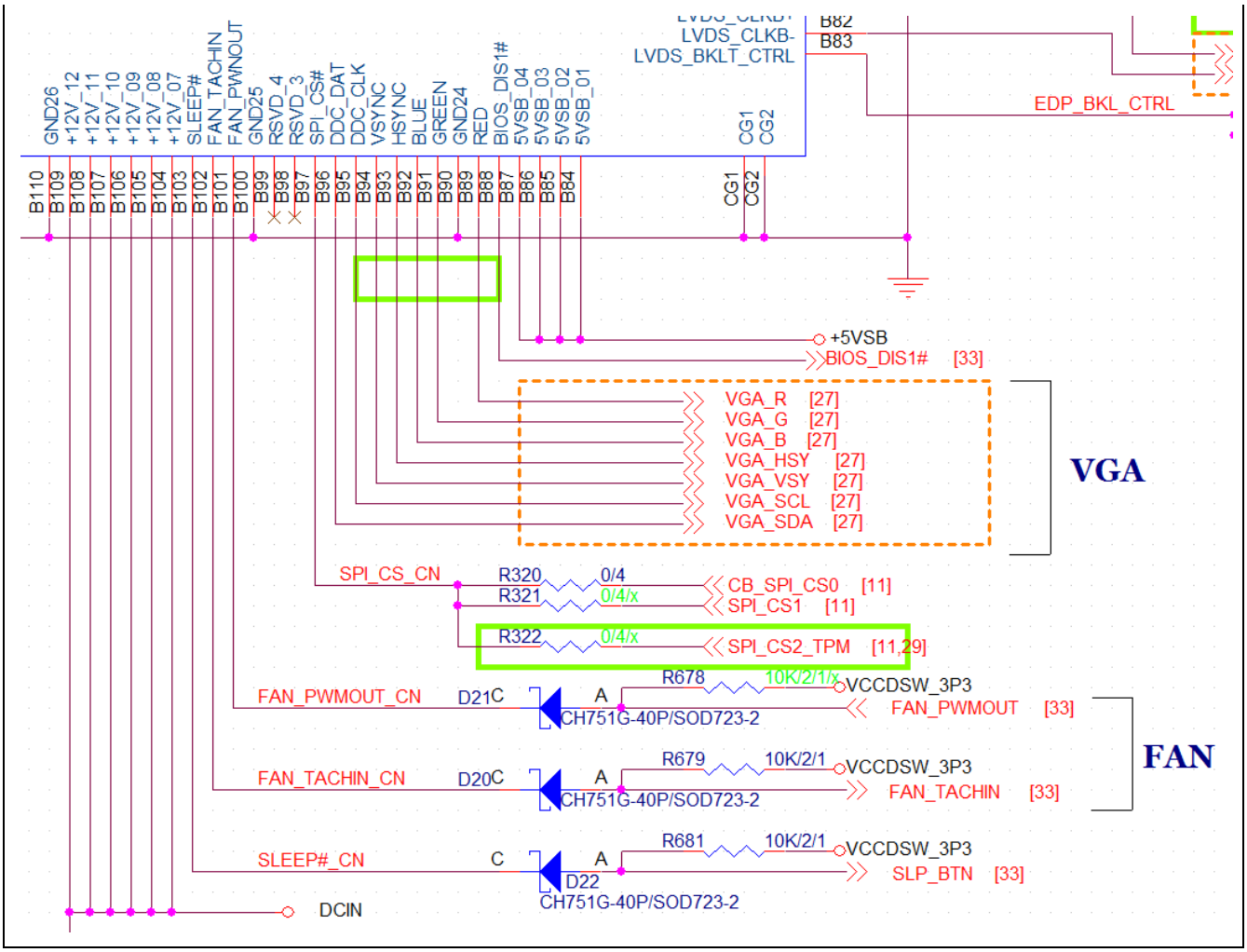


Figure 19 Circuit protection on Module

6.2 Carrier protection

Avoiding Carrier accidentally exposure to VCC_12V pool, a circuit protection design should be implemented on the Carrier, please refer to Fig.21 Carrier circuit protection schematic.

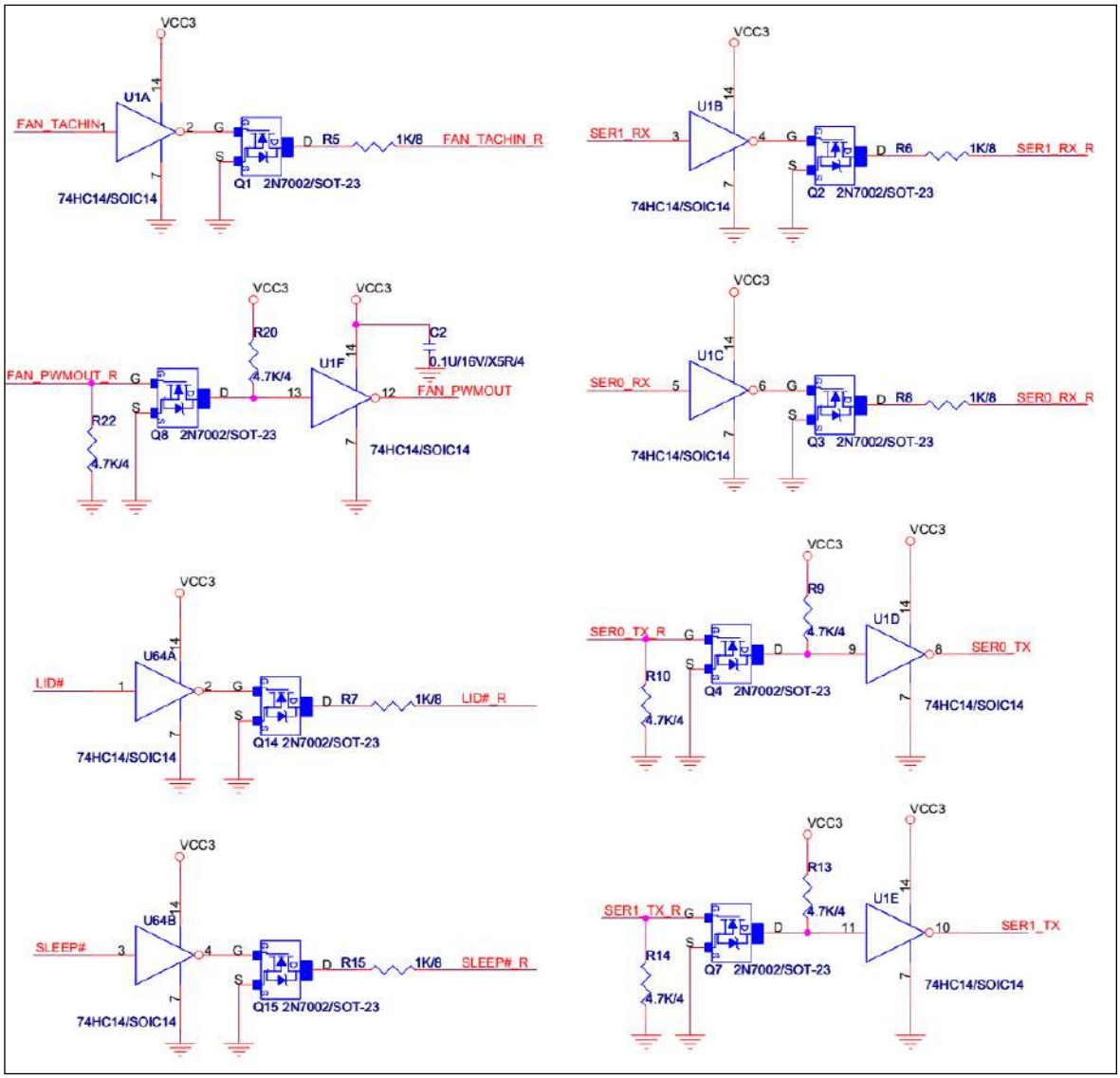


Figure 20 Circuit protection on Carrier

7 Industry Specifications

1. Low Pin Count Interface Specification, Revision 1.0 (LPC)
   http://www.intel.com/design/chipsets/industry/lpc.htm
2. Universal Serial Bus (USB) Specification, Revision 2.0
   http://www.usb.org/home
3. Serial ATA Specification, Revision 3.0
   http://www.serialata.org/
4. PCI Express Base Specification, Revision 2.0
   https://www.pcisig.com/specifications
5. PICMG® COM Express Module™ Base Specification
   http://www.picmg.org/
6. PICMG®COM Express Carrier Board Design Guide
   http://www.picmg.org/