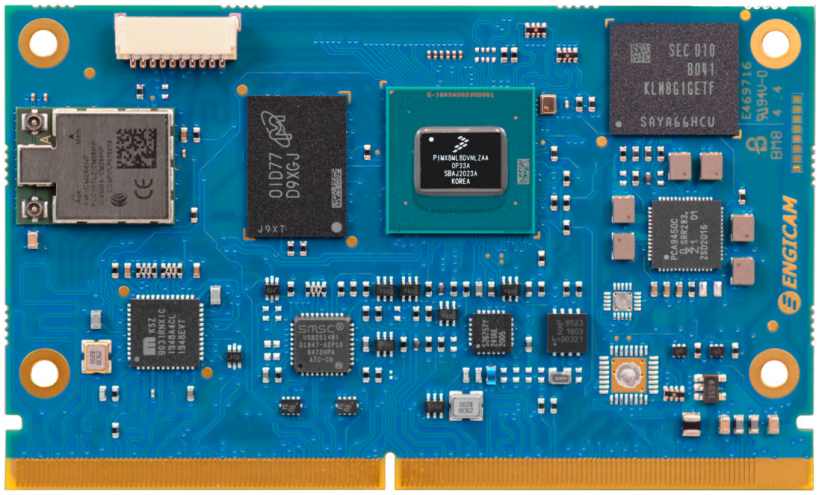
SmarCore MX8M Plus HW manual 1.0.0



SMARC Version 2.1 Compliant

Standardization Group for Embedded Technologies
SGeT
Member

Revision history

DATE	REVISION	CHANGE DESCRIPTION
11/02/2021	1.0.0	Release

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Chapter

1

1. Introduction

This Chapter gives background information on this document.
Section includes：

- **Acronyms and Abbreviations Used**
- **Signal Table Terminology**
- **Document and Standard References**

This document is created to guide users to design SMARC compliant carrier board. It will focus only on the interfaces in SMARC MX8M Plus pinout and related peripherals. Some interfaces defined in SMARC specification, but not in SMARC MX8M Plus, will not be addressed in this document.

This document also contains reference schematics for different interfaces.

SMARC MX8M Plus module does not feature the full set of all interfaces that defined in SMARC specification.

This document helps walk hardware designers through the various stages of designing a carrier board on this platform. Using this document, hardware designers can efficiently locate the resources they need at every step in the board design flow.

An evaluation carrier is available for SMARC MX8M Plus computer on module.

All examples of this document are based on SMARC MX8M Plus carrier board that is available from ENGICAM. This document also provides a collection of useful documentation, application reports, and design recommendations.

1.1 Acronyms and Abbreviations used

The table below shows the acronyms and abbreviations used in the manual.

ABBREVIATION	EXPLANATION
ADC	Analogue to Digital Converter
Auto-MDIX	Automatically Medium Dependent Interface Crossing, a PHY with Auto-MDIX f is able to detect whether RX and TX need to be crossed (MDI or MDIX)
CAN	Controller Area Network, a bus that is manly used in automotive and industrial environment
CPU	Central Processor Unit
DAC	Digital to Analogue Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor
DSI	Display Serial Interface
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high frequency disturbances
eMMC	Embedded Multi Media Card, flash memory combined with MMC interface controller in a BGA package, used as internal flash memory
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GPIO	General Purpose Input/Output, pin that can be configured being an input or output
HDA	High Definition Audio (HD Audio), digital audio interface between CPU and audio codec
HDMI	High-Definition Multimedia Interface, combines audio and video signal
I2C	Inter-Integrated Circuit, two wire interfaces for connecting low speed peripherals
I2S	Integrated Interchain Sound, serial bus for connecting PCM audio data between two devices

ABBREVIATION	EXPLANATION
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signalling, electrical interface standard that can transport very high speed signals over twisted-pair cables.
MSB	Most Significant Bit
NA	Not Available
NC	Not Connected
OD	Open Drain
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PD	Pull Down Resistor
PHY	Physical Layer of the OSI model
PMIC	Power Management IC, integrated circuit that manages amongst others the power sequence of a system
PU	Pull Up Resistor
PWM	Pulse-Width Modulation
RGB	Red Green Blue, colour channels in common display interfaces
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SOC	System on a Chip, IC which integrates the main component of a computer on a single chip
SPI	Serial Peripheral Interface Bus, synchronous four wire full duplex bus for peripherals
USB	Universal Serial Bus, serial interface for internal and external peripherals

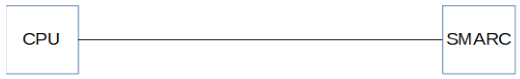
1.2 Signal Table Terminology

The Table below describes the terminology used in this section for the Signal Description tables.

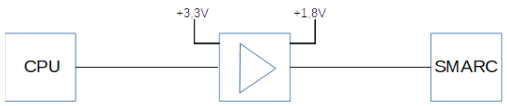
The “#” symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When “#” is not present, the signal is asserted when at a high voltage level.

DIRECTION	TYPE	NOTE
Input		Input to the Module
Output		Output from the Module
Output OD		Open drain output from the Module
Bi-Dir		Bi-directional signal (can be input or output)
Bi-Dir OD		Bi-directional signal; output from the Module is open drain
Diff100		Differential 100 Ohm
Diff90		Differential 90 Ohm
	VDD_IN	Module input voltage
	CMOS 1.8V	CMOS logic input and / or output, 1.8V I/O supply level or tolerance
	CMOS 3.3V	CMOS logic input and / or output, 3.3V I/O supply level or tolerance
	CMOS VDD_IO	CMOS logic I/O level – set to 1.8V for SMARC MX8M Plus
	CMOS VDD_JTAG_IO	VDD_JTAG_IO is 1.8V in SMARC MX8M Plus. The JTAG emulator adjusts to the VDD_JTAG_IO level provided by the Module, on the JTAG connector
	GBE MDI	Differential analog signalling for Gigabit Media Dependent Interface
	LVDS AFB	LVDS signalling for AFB – may be PCIe, SATA, USB SS, GBE MDI, MLB or other low voltage high speed differential physical interface

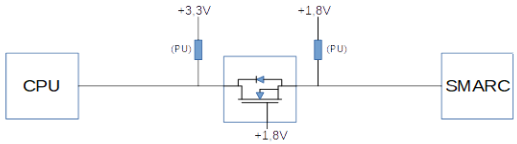
Schematics reference for GPIO configurations and level translation



GPIO Capable



Output signal



GPIO LTD (PU value)

1.3 Document and Standard References

1.3.1 External Industry Standard Documents

- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com).
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com).
- MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org).
- PICMG® EEEP Embedded EEPROM Specification, Rev. 1.0, August 2010 (www.picmg.org).
- SD Specifications Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org).
- SPI Bus – "Serial Peripheral Interface" - de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus).
- USB Specifications (www.usb.org).

1.3.2 SGET Documents

SMARC_Hardware_Specification version 2.1, March 23, 2020.

1.4 Non-intended use

WARNING

Use the SMARC module in the specified temperature ranges only!

Use the SMARC module in the specified humidity ranges only!

1.5 Electrostatic Sensitive Device

The ENGICAM SMARC module is an electrostatic sensitive device and it is packed accordingly.

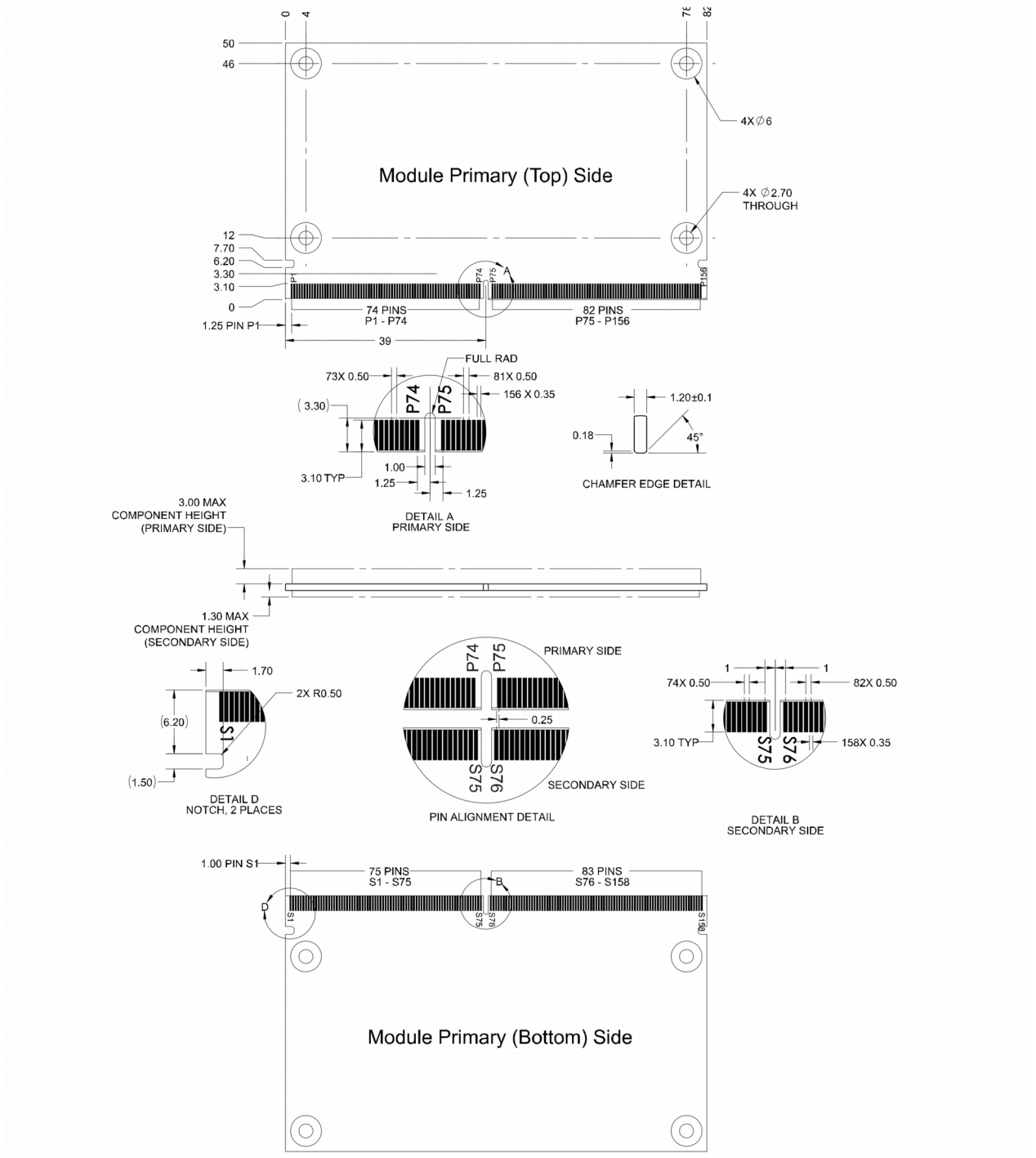
Warning:

Handle the SMARC Module at electrostatic-free workstations only.

Do not handle or store the SMARC Module near strong electrostatic, electromagnetic, magnetic or radioactive fields unless the SMARC Module is contained within its original packaging.

1.6 Mechanical definitions

Engicam SMARC module respects SGET SMARC mechanical definitions. Figure below comes from SMARC_Hardware_Specification version 2.0, June 2, 2016.



Chapter

2

2. Ordering Information

This Chapter gives the ordering information and technical specifications of the modules.

Section includes:

- **Ordering code**
- **CPU & Memory specifications**
- **Operating temperature range**

2.1 Ordering Information

Following are provided the ordering information and the description of the basic technical specifications for the modules:

Marking Code	Ordering Code	MPQ	Description	CPU & Memory specifications	Operating temperature range °C (excepted CPU)[2]	Module available at least until [1]
SMARCORE MX8M Plus	**002680023QI550**	1	SMARC 2.0 short size iMX8M Plus, 2GB LPDDR4, 8GB **eMMC -25°C**, dual GB Ethernet, No WiFi, Industrial.	i.MX8M Plus Quad Industrial Temperature **MIMX8ML8CVNKZAB** 1.8 GHz Industrial GPU/VPU, -40 to +105 °C [2] 32 bit LPDDR4 @ 4000MTs, temperature range Industrial	-40 to +85	1th Q - 2031
SMARCORE MX8M Plus	**002670023QI550**	58	SMARC 2.0 short size iMX8M Plus, 2GB LPDDR4, 8GB **eMMC -25°C**, dual GB Ethernet, No WiFi, Industrial.		-40 to +85	1th Q - 2031

Following are provided the ordering information and the description for the module's Starterkit:

Marking Code	Ordering Code	MPQ	Description	Operating temperature range °C (excepted CPU)[2]
SmarCore MX8M Plus STARTERKIT	0026K0023QI550	1	**module included: SMARCORE MX8M Plus, 2GB LPDDR, 8GB eMMC -25°C, Industrial**	-40 to +85

[1] **Long Term Availability based on NXP longevity program**

[2] ***Note: internal junction temperature***

WARNING: the temperature depend on the application, the enclosure and/or the environmental condition. Upon customer to consider specific cooling solutions for its own final system.

Chapter

3

3. Pinout and Futures

Section includes:

- **Pinout overview**
- **SMARC supported futures**

3.1 Module pinout compared with full set SMARC

There are 314 edge fingers of the SMARC module that mate with a low profile 314 pin 0.5mm pitch right angle connector. The following table lists the module pin assignments for all 314 edge fingers.

SMARCORE MX8M Plus match SMARC specifications V.2P1

P-Pin	SIGNAL	V Rail	GPIO	S-Pin	SIGNAL	V Rail	GPIO
				S1	I2C_CAM1_CK	+1,8V	Y
P1	SMB_ALERT_1V8#	-	-	S2	I2C_CAM1_DAT	+1,8V	Y
P2	GND	-	-	S3	GND	-	-
P3	CSI1_CK+	+1,8V	Y	S4	RSVD	-	-
P4	CSI1_CK-	+1,8V	Y	S5	I2C_CAM0_CK	+1,8V	Y
P5	GBE1_SDP	-	-	S6	CAM_MCK	+1,8V	Y
P6	GBE0_SDP	+3,3V	-	S7	I2C_CAM0_DAT	+1,8V	Y
P7	CSI1_RX0+	+1,8V	Y	S8	CSI0_CK+	+1,8V	Y
P8	CSI1_RX0-	+1,8V	Y	S9	CSI0_CK-	+1,8V	Y
P9	GND	-	-	S10	GND	-	-
P10	CSI1_RX1+	+1,8V	Y	S11	CSI0_D0+	+1,8V	Y
P11	CSI1_RX1-	+1,8V	Y	S12	CSI0_D0-	+1,8V	Y
P12	GND	-	-	S13	GND	-	-
P13	CSI1_RX2+	+1,8V	Y	S14	CSI0_D1+	+1,8V	Y
P14	CSI1_RX2-	+1,8V	Y	S15	CSI0_D1-	+1,8V	Y
P15	GND	-	-	S16	GND	-	-
P16	CSI1_RX3+	+1,8V	Y	S17	GBE1_MDI0+	-	N
P17	CSI1_RX3-	+1,8V	Y	S18	GBE1_MDI0-	-	N
P18	GND	-	-	S19	GBE1_LINK100#	-	N
P19	GBE_MDI3-	-	N	S20	GBE1_MDI1+	-	N
P20	GBE_MDI3+	-	N	S21	GBE1_MDI1-	-	N
P21	GBE_LINK100#	-	N	S22	GBE1_LINK1000#		
P22	GBE_LINK1000#	3,3V PU	N	S23	GBE1_MDI2+	-	N
P23	GBE_MDI2-	-	N	S24	GBE1_MDI2-	-	N
P24	GBE_MDI2+	-	N	S25	GND	-	-
P25	GBE_LINK_ACT#	-	N	S26	GBE1_MDI3+	-	N
P26	GBE_MDI1-	-	N	S27	GBE1_MDI3-	-	N
P27	GBE_MDI1+	-	N	S28	GBE1_CTREF+	-	-
P28	GBE_CTREF	-	-	S29	PCIE_D_TX+	-	-
P29	GBE_MDI0-	-	N	S30	PCIE_D_TX-	-	-
P30	GBE_MDI0+	-	N	S31	GBE1_LINK_ACT#	-	N
P31	SPI0_CS1#	+1,8V	Y	S32	PCIE_D_RX+	-	-
P32	GND	-	-	S33	PCIE_D_RX-	-	-
P33	SDIO_WP	+3,3V	Y	S34	GND	-	-
P34	SDIO_CMD	+3,3V	Y	S35	USB4+	USB	N
P35	SDIO_CD#	+3,3V	Y	S36	USB4-	USB	N
P36	SDIO_CK	+3,3V	Y	S37	USB3_VBUS_DET	-	-
P37	SDIO_PWR_EN	+3,3V	Y	S38	AUDIO_MCK	+1,8V	Y
P38	GND	-	-	S39	I2S0_LRCK	+1,8V	Y
P39	SDIO_D0	+3,3V	Y	S40	I2S0_SDOUT	+1,8V	Y
P40	SDIO_D1	+3,3V	Y	S41	I2S0_SDIN	+1,8V	Y
P41	SDIO_D2	+3,3V	Y	S42	I2S0_CK	+1,8V	Y

P-Pin	SIGNAL	V Rail	GPIO	S-Pin	SIGNAL	V Rail	GPIO
P42	SDIO_D3	+3,3V	Y	S43	ESPI_ALERT0#	+1,8V	Y
P43	SPI0_CS0#	+1,8V	Y	S44	ESPI_ALERT1#	+1,8V	Y
P44	SPI0_CK	+1,8V	Y	S45	RSVD	-	-
P45	SPI0_DIN	+1,8V	Y	S46	RSVD	-	-
P46	SPI0_DO	+1,8V	Y	S47	GND	-	-
P47	GND	-	-	S48	I2C_GP_CK	+1,8V	GPIO LTD(3K3)
P48	SATA_TX+	-	-	S49	I2C_GP_DAT	+1,8V	GPIO LTD(3K3)
P49	SATA_TX-	-	-	S50	HDA_SYNC	-	-
P50	GND	-	-	S51	HDA_SDO	-	-
P51	SATA_RX+	-	-	S52	HDA_SDI	-	-
P52	SATA_RX-	-	-	S53	HDA_CK	-	-
P53	GND	-	-	S54	SATA_ACT#	-	-
P54	ESPI_CS0#	+1,8V	Y	S55	USB5_EN_OC#	-	-
P55	ESPI_CS1#	+1,8V	Y	S56	ESPI_IO_2	+1,8V	Y
P56	ESPI_CK	+1,8V	Y	S57	ESPI_IO_3	+1,8V	Y
P57	ESPI_IO_1	+1,8V	Y	S58	ESPI_RESET	-	-
P58	ESPI_IO_0	+1,8V	Y	S59	USB5+	-	-
P59	GND	-	-	S60	USB5-	-	-
P60	USB0+	USB	N	S61	GND	-	-
P61	USB0-	USB	N	S62	USB3_SSTX+	USB	N
P62	USB0_EN_OC#	+3,3V	Y	S63	USB3_SSTX-	USB	N
P63	USB0_VBUS_DET	+3,3V	Y	S64	GND	-	-
P64	USB0_OTG_ID	+3,3V	Y	S65	USB3_SSRX+	USB	N
P65	USB1+	USB	N	S66	USB3_SSRX-	USB	N
P66	USB1-	USB	N	S67	GND	-	-
P67	USB1_EN_OC#	+3,3V	N	S68	USB3+	USB	N
P68	GND	-	-	S69	USB3-	USB	N
P69	USB2+	USB	N	S70	GND	-	-
P70	USB2-	USB	N	S71	USB2_SSTX+	USB SS	N
P71	USB2_EN_OC#	+3,3V	N	S72	USB2_SSTX	USB SS	N
P72	RSVD	-	-	S73	GND	-	-
P73	RSVD	-	-	S74	USB2_SSRX+	USB SS	N
P74	USB3_EN_OC#	+3,3V	N	S75	USB2_SSRX-	USB SS	N
	<KEY>				<KEY>		
P75	PCIE_A_RST#	+3,3V	Y	S76	PCIE_B_RST#	-	-
P76	USB4_EN_OC#	+3,3V	N	S77	PCIE_C_RST#	-	-
P77	PCIE_B_CKREQ#	-	-	S78	PCIE_C_RX+	-	-
P78	PCIE_A_CKREQ#	+1,8V	N	S79	PCIE_C_RX-	-	-
P79	GND	-	-	S80	GND	-	-
P80	PCIE_C_REFCK+	-	-	S81	PCIE_C_TX+	-	-
P81	PCIE_C_REFCK-	-	-	S82	PCIE_C_TX-	-	-
P82	GND	-	-	S83	GND	-	-
P83	PCIE_A_REFCK+	+1,8V	N	S84	PCIE_B_REFCK+	-	-
P84	PCIE_A_REFCK-	+1,8V	N	S85	PCIE_B_REFCK-	-	-
P85	GND	-	-	S86	GND	-	-
P86	PCIE_A_RX+	+1,8V	N	S87	PCIE_B_RX+	-	-
P87	PCIE_A_RX-	+1,8V	N	S88	PCIE_B_RX-	-	-
P88	GND	-	-	S89	GND	-	-

P-Pin	SIGNAL	V Rail	GPIO	S-Pin	SIGNAL	V Rail	GPIO
P89	PCIE_A_TX+	+1,8V	N	S90	PCIE_B_TX+	-	-
P90	PCIE_A_TX-	+1,8V	N	S91	PCIE_B_TX-	-	-
P91	GND	-	-	S92	GND	-	-
P92	HDMI_D2+ / DP1_LANE0+	-	-	S93	DP0_LANE0+	-	-
P93	HDMI_D2- / DP1_LANE0-	-	-	S94	DP0_LANE0-	-	-
P94	GND	-	-	S95	DP0_AUX_SEL	-	-
P95	HDMI_D1+ / DP1_LANE1+	-	-	S96	DP0_LANE1+	-	-
P96	HDMI_D1- / DP1_LANE1-	-	-	S97	DP0_LANE1-	-	-
P97	GND	-	-	S98	DP0_HPD	-	-
P98	HDMI_D0+ / DP1_LANE2+	-	-	S99	DP0_LANE2+	-	-
P99	HDMI_D0- / DP1_LANE2-	-	-	S100	DP0_LANE2-	-	-
P100	GND			S101	GND	-	-
P101	HDMI_CK+ / DP1_LANE3+	-	-	S102	DP0_LANE3+	-	-
P102	HDMI_CK- / DP1_LANE3+	-	-	S103	DP0_LANE3-	-	-
P103	GND	-	-	S104	USB3_OTG_ID	+3,3V	N
P104	HDMI_HPD / DP1_HPD			S105	DP0_AUX+	-	-
P105	HDMI_CTRL_CK / DP1_AUX+	-	-	S106	DP0_AUX-	-	-
P106	HDMI_CTRL_DAT / DP1_AUX-	-	-	S107	LCD1_BKLT_EN	+1,8V	Y
P107	DP1_AUX_SEL	-	-	S108	LVDS1_CK+	+2,5V	N
P108	GPIO0/CAM0_PWR#	+1,8V	Y	S109	LVDS1_CK-	+2,5V	N
P109	GPIO1/CAM1_PWR#	+1,8V	Y	S110	GND	-	-
P110	GPIO2/CAM0_RST#	+1,8V	Y	S111	LVDS1_0+	+2,5V	N
P111	GPIO3/CAM1_RST#	+1,8V	Y	S112	LVDS1_0-	+2,5V	N
P112	GPIO4/HDA_RST#	+1,8V	Y	S113	eDP1_HPD	-	-
P113	GPIO5/PWM_OUT	+1,8V	Y	S114	LVDS1_1+	+2,5V	N
P114	GPIO6/TACHIN	+1,8V	Y	S115	LVDS1_1-	+2,5V	N
P115	GPIO7	+1,8V	Y	S116	LCD1_VDD_EN	-	-
P116	GPIO8	+1,8V	Y	S117	LVDS1_2+	+2,5V	N
P117	GPIO9	+1,8V	Y	S118	LVDS1_2-	+2,5V	N
P118	GPIO10	+1,8V	Y	S119	GND	-	-
P119	GPIO11	+1,8V	Y	S120	LVDS1_3+	+2,5V	N
P120	GND	-	-	S121	LVDS1_3-	+2,5V	N
P121	I2C_PM_CK	+1,8V	Y	S122	LCD1_BKLT_PWM	+1,8V	Y
P122	I2C_PM_DAT	+1,8V	Y	S123	GPI=13	-	-
P123	BOOT_SEL0#	-	-	S124	GND	-	-
P124	BOOT_SEL1#	+1,8V	N	S125	LVDS0_0+	+2,5V	N
P125	BOOT_SEL2#	-	-	S126	LVDS0_0-	+2,5V	N
P126	RESET_OUT#	+1,8V	N	S127	LCD_BKLT_EN	+1,8V	Y
P127	RESET_IN#	+1,8V	N	S128	LVDS0_1+	+2,5V	N
P128	POWER_BTN#	+1,8V	N	S129	LVDS0_1-	+2,5V	N
P129	SER0_TX	+1,8V	Y	S130	GND	-	-
P130	SER0_RX	+1,8V	Y	S131	LVDS0_2+	+2,5V	N
P131	SER0_RTS#	+1,8V	Y	S132	LVDS0_2-	+2,5V	N
P132	SER0_CTS#	+1,8V	Y	S133	LCD_VDD_EN	+1,8V	Y
P133	GND	-	-	S134	LVDS0_CK+	+2,5V	N
P134	SER1_TX	+1,8V	Y	S135	LVDS0_CK-	+2,5V	N
P135	SER1_RX	+1,8V	Y	S136	GND	-	-
P136	SER2_TX	+1,8V	Y	S137	LVDS0_3+	+2,5V	N

P-Pin	SIGNAL	V Rail	GPIO	S-Pin	SIGNAL	V Rail	GPIO
P137	SER2_RX	+1,8V	Y	S138	LVDS0_3-	+2,5V	N
P138	SER2_RTS#	+1,8V	Y	S139	I2C_LCD_CK	+1,8V	Y
P139	SER2_CTS#	+1,8V	Y	S140	I2C_LCD_DAT	+1,8V	Y
P140	SER3_TX	+1,8V	Y	S141	LCD_BKLT_PWM	+1,8V	Y
P141	SER3_RX	+1,8V	Y	S142	GPIO12	+1,8V	Y
P142	GND	-	-	S143	GND	-	-
P143	CAN0_TX	+1,8V	Y	S144	EDP0_HPD	+1,8V	Y
P144	CAN0_RX	+1,8V	Y	S145	WDT_TIME_OUT#	-	-
P145	CAN1_TX	+1,8V	Y	S146	PCIE_WAKE#	+3,3V	Y
P146	CAN1_RX	+1,8V	Y	S147	VDD_RTC	+3,3V	-
P147	VDD_IN	+5V in	-	S148	LID#	+1,8V	Y
P148	VDD_IN	+5V in	-	S149	SLEEP#	+1,8V	Y
P149	VDD_IN	+5V in	-	S150	VIN_PWR_BAD#	+3,3V	N
P150	VDD_IN	+5V in	-	S151	CHARGING#	+1,8V	Y
P151	VDD_IN	+5V in	-	S152	CHARGER_PRSNT#	+1,8V	Y
P152	VDD_IN	+5V in	-	S153	CARRIER_STBY#	+1,8V	N
P153	VDD_IN	+5V in	-	S154	CARRIER_PWR_ON	+1,8V	N
P154	VDD_IN	+5V in	-	S155	FORCE_RECOV#	+1,8V	N
P155	VDD_IN	+5V in	-	S156	BATLOW#	+1,8V	Y
P156	VDD_IN	+5V in	-	S157	TEST#		
				S158	GND	-	-

Note:

The text in grey represents the signals defined in SMARC specification, but not implemented in SMARC MX8M Plus.

3.2 SMARC supported futures

The following table summarizes the SMARC features implemented on SMARC MX8M Plus compared with the standard specifications.

All mandatory features required by the SMARC specification are implemented in the SMARC MX8M Plus Module.

Feature	Sub Feature	Mandatory	SMARC MX8M Plus implementation	Note
Parallel LCD	24 bit Parallel RGB interface	No	No	
LVDS LCD	18 bit single channel	No	Yes	
	24 bit single channel – 18 bit compatible	No	Yes	
	24 bit single channel – standard color map	No	Yes	
	Clock for dual channel support	No	Yes	
HDMI	HDMI display interface	No	Yes	
	HDMI CEC function	No	Yes	
Camera	CSI0 – 2 lane	No	Yes	

Feature	Sub Feature	Mandatory	SMARC MX8M Plus implementation	Note
	CSI1 – 2 lane implementation	No	Yes	
	CSI1 – 4 lane implementation	No	Yes	
SDIO	SDIO (4 bit, for SD cards)	Yes	Yes	
SDMMC	SDMMC (8 bit, eMMC capable)	No	Yes	
SPI	SPI0	No	Yes	
	SPI1	No	Yes	
I2S	I2S0	Yes	Yes	
	I2S1	No	No	
	I2S2	No	No	
	I2S2 – HDA variant	No	No	
I2C	Power Management	Yes	Yes	
	General Purpose	Yes	Yes	
	Camera	No	Yes	
	LCD (Parallel or LVDS) Display I/D	No	Yes	
Serial Ports	SER0 (4 wire)	Yes	Yes	
	SER1 (2 wire)	Yes	Yes	
	SER2 (4 wire)	No	Yes	
	SER3 (2 wire)	No	Yes	
CAN Bus	CAN0	No	Yes	
	CAN1	No	Yes	
USB	USB0 - as USB 2.0 Client	Yes	Yes	
	USB0 - as USB 2.0 Host / OTG	Yes	Yes	
	USB1 - as USB 2.0 Host	Yes	Yes	
	USB2 – as USB 2.0 Host	No	Yes	
PCIe	PCIE_A (x1 Gen 1 Root)	No	Yes	
	PCIE_B (x1 Gen 1 Root)	No	No	
	PCIE_C (x1 Gen 1 Root)	No	No	
	PCIE Gen 2 operation	No	No	
SATA	SATA Gen 1	No	No	
	SATA Gen 2 operation	No	No	
	SATA Gen 3 operation	No	No	
GBE	Gigabit Ethernet	No	Yes x2	

Feature	Sub Feature	Mandatory	SMARC MX8M Plus implementation	Note
SPDIF		No	No	
Watchdog	WDT Out	No	No	
GPIO	GPIOs – 12x	Yes	Yes	
	GPIO interrupt capability – 12x	Yes	Yes	
	GPIO Camera Support	Yes	Yes	
	GPIO5 PWM capability	No	No	
	GPIO6 Tachin capability	No	No	
Management	System and power management features	Yes	Yes	
Boot Select		Yes	Yes	
Force Recov		No	No	
JTAG	JTAG connector on Module	No	No	

Chapter

4

4. Power Supply

Section includes:

- **Power signals**
- **VDDIO Voltage Rail**
- **RTC battery**
- **Control signals and power sequences**
- **Boot modes**
- **Power states**
- **Watchdog**

4.1 Power Signals

Read carefully the related sections before starting your power stage design. This module needs to be supplied up to +5Vin power. Refer to the table below for the power supply range specification.

Note: the system must provide at least a power of 2A at 5V to allow the start of the module.

	Min	Typ	Max
Voltage range	+4,9V	+5V	+5,25V
Module Current working mode	-	tbd mA	-
Module Current in standby mode		tbd mA	

Table

Note: *the measures in the table above are to be considered referred to the module with only the Linux OS running once loaded (during the OS transient load can reach also 600 mA), the use of graphic accelerators or other multimedia applications could be caused of higher consumption than those indicated.*

In the following table are shown the module power supply pins numbering, connect all power supply pins in order to avoid damage.

P-Pin	Name	Primary Function Description	S-Pin	Name	Primary Function Description
P2	GND	Power return-Ground reference	S3	GND	Power return-Ground reference
P9	GND	Power return-Ground reference	S10	GND	Power return-Ground reference
P12	GND	Power return-Ground reference	S13	GND	Power return-Ground reference
P15	GND	Power return-Ground reference	S16	GND	Power return-Ground reference
P18	GND	Power return-Ground reference	S25	GND	Power return-Ground reference
P32	GND	Power return-Ground reference	S34	GND	Power return-Ground reference
P38	GND	Power return-Ground reference	S47	GND	Power return-Ground reference
P47	GND	Power return-Ground reference	S61	GND	Power return-Ground reference
P50	GND	Power return-Ground reference	S64	GND	Power return-Ground reference
P53	GND	Power return-Ground reference	S67	GND	Power return-Ground reference
P59	GND	Power return-Ground reference	S70	GND	Power return-Ground reference
P68	GND	Power return-Ground reference	S73	GND	Power return-Ground reference
<KEY>					
P79	GND	Power return-Ground reference	S80	GND	Power return-Ground reference
P82	GND	Power return-Ground reference	S83	GND	Power return-Ground reference
P85	GND	Power return-Ground reference	S86	GND	Power return-Ground reference
P88	GND	Power return-Ground reference	S89	GND	Power return-Ground reference
P91	GND	Power return-Ground reference	S92	GND	Power return-Ground reference
P94	GND	Power return-Ground reference	S101	GND	Power return-Ground reference
P97	GND	Power return-Ground reference	S110	GND	Power return-Ground reference
P100	GND	Power return-Ground reference	S119	GND	Power return-Ground reference

P-Pin	Name	Primary Function Description	S-Pin	Name	Primary Function Description
P103	GND	Power return-Ground reference	S124	GND	Power return-Ground reference
P120	GND	Power return-Ground reference	S130	GND	Power return-Ground reference
P133	GND	Power return-Ground reference	S136	GND	Power return-Ground reference
P142	GND	Power return-Ground reference	S143	GND	Power return-Ground reference
P147	VDD_IN	Power input voltage-5.0V (5.25V Max)			
P148	VDD_IN	Power input voltage-5.0V (5.25V Max)			
P149	VDD_IN	Power input voltage-5.0V (5.25V Max)			
P150	VDD_IN	Power input voltage-5.0V (5.25V Max)			
P151	VDD_IN	Power input voltage-5.0V (5.25V Max)			
P152	VDD_IN	Power input voltage-5.0V (5.25V Max)			
P153	VDD_IN	Power input voltage-5.0V (5.25V Max)			
P154	VDD_IN	Power input voltage-5.0V (5.25V Max)			
P155	VDD_IN	Power input voltage-5.0V (5.25V Max)			
P156	VDD_IN	Power input voltage-5.0V (5.25V Max)			

Table 6

Only +5V power support

4.2 VDDIO Voltage Rail

The module is compliant to SMARC_Hardware_Specification_V2.1.

For details refer to SMARC_Hardware_Specification_V2.1 and Chapter 5 of this document.

4.3 RTC battery

The standard provides a signal to power supply a RTC on module. If not used this pin may be left floating.

Pin	Name	Type / Tolerance	Use
S147	VDD_RTC	Power In	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap.
		Power Out (when charging a Super Cap)	The connection with module is obtained by connecting directly the backup battery to the VDD_RTC signal. **Note:** *The module is already designed to manage the charge of backup battery, by a siple 1KOhm series resistor from 3.1V.*

Optional RTC on board

4.4 Control signals and power sequences

The module signal CARRIER_PWR_ON exists to ensure that the module is powered before the main body of carrier circuits. The carrier system should not be powered until the module asserts the CARRIER_PWR_ON signal as a high. The hardware of module should assert CARRIER_PWR_ON when all the module's supplies necessary for module booting are up. The module should continue to assert the signal RESET_OUT# after the release of CARRIER_PWR_ON, for a period enough to allow to the carrier power circuits to come up.

PIN	NAME	CPU PIN NAME	DIRECTION	RAIL	Function Description
S154	PGOOD	-	OUT	+1.8V	Carrier power enable from module
S150	VIN_PWR_BAD#	-	IN	+1.8V	Power bad indication from carrier
S153	CARRIER_STBY#	-	OUT	+1.8V	Drive low by module during standby
P126	RESET_OUT#	POR_B	OUT	+1.8V	Reset Output to carrier
P127	RESET_IN#		IN	+1.8V	Reset Input from carrier
P128	POWER_BTN#	ON_OFF_BUTT	IN	+1.8V	Power button Input from carrier
S149	SLEEP#	CSID00	IN	+1.8V	Sleep indicator from carrier (NOT available)
S148	LID#	CSID01	IN	+1.8V	Lid open/close indication
S156	BATLOW#	ADC_IN0	IN	+1.8V	Battery low indication
P122	I2C_PM_DAT	CSI_RESET	BI-DIR	+1.8V	Power management I2C bus data
P121	I2C_PM_CK	CSI_EN	BI-DIR	+1.8V	Power management I2C bus clock
S151	CHARGING#	ADC_IN2	IN	+1.8V	Charge indicator (low during the charging)
S152	CHARGER_PRSNT#	ADC_IN1	IN	+1.8V	Charger present
S157	TEST#	NC	IN	-	
S155	FORCE_RECOV	SCU_BOOT_MODE1	IN	+1.8V	

Note: refer to SMARC_Hardware_Specification version 2.1 for details

I2C_PM address 1101000 is reserved for the PCIe CLK Generator and RTC and calendar IC 1101 0001

4.5 Boot modes

The SMARC MX8M Plus performs the bootstrap using the signals nSD_BOOT (P124) and nBOOT_MODE (S155) according to the following table

nSD_BOOT	nBOOT_MODE	BOOT Source
X	GND	SERIAL DOWNLOAD
GND	OPEN	SD CARD
OPEN	OPEN	eMMC

When pin 155 is tied to GND, the CPU enter in "serial download mode", in this mode the CPU can be driven by NXP PC software tools. Engicam suggests to leave this pin open because NXP tools are not so easy to use, they need serial, USB OTG and needs drivers for the SOM.

When pin P124 is tied to GND, the CPU enter in "SD card boot mode", in this mode the CPU can boot from the SD card on the carrier. This mode can easily be used for module re-programming from scratch, and we suggest to provide a jumper to GND on this pin or something similar.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	Function Description
P124	nSD_BOOT	SCU_BOOT_MODE0	N	+1,8V	Input signals that determine the Module's boot device. Pulled up on Module – 3K3 Ohm
S155	nBOOT_MODE	SCU_BOOT_MODE1	N	+1,8V	

4.6 Power states

The SMARC module supports different power states. In the table below are described the behaviour in the different states.

STATUS	Module Status	Carrier Status	Status Description
Unplugged			No power is applied to the system, except the RTC battery might be available (if used)
Off			System is off, but the carrier board input supply is available
Suspend	The module is in the standby mode all the features are off except the wakeup capable one	All the power rails are available, while the peripherals are stopped via software	System is suspended and waits for a wakeup source
Run	CPU is available at 100%	All power rails are on and all the peripherals and CPU features are available	System is running
Reset	All the CPU features are in reset mode, power rails are on	All the peripherals are in reset mode, power rails are on	System is put in reset state by holding RESET_IN# is low

Chapter

5

5. Interfaces

Section includes:

- **Ethernet**
- **USB**
- **LVDS**
- **SDIO**
- **I2S**
- **SPI**
- **SERIALS**
- **CAN**
- **PCIe**
- **GPIO**
- **CAMERA INTERFACE**
- **CONTROLS**

5.1 Ethernet

SMARC MX8M Plus Module support up to 2 Gigabit Ethernet interfaces. This means that the customer has the possibility to have two autonomous Ethernet with two independent IP address. The following table describes primary GBE signals organization.

PIN	NAME	PHY PIN NAME	NOTE
P29	GBE_MDI0-	ETH_TXRXM_A	Diff100
P30	GBE_MDI0+	ETH_TXRXP_A	
P26	GBE_MDI1-	ETH_TXRXM_B	Diff100
P27	GBE_MDI1+	ETH_TXRXP_B	
P23	GBE_MDI2-	ETH_TXRXM_C	Diff100
P24	GBE_MDI2+	ETH_TXRXP_C	
P19	GBE_MDI3-	ETH_TXRXM_D	Diff100
P20	GBE_MDI3+	ETH_TXRXP_D	
P21	GBE_LINK100#	-	Output OD (12mA)
P22	GBE_LINK1000#	-	Output OD (12mA)
P25	GBE_LINK_ACT#	-	Output OD (12mA)

The secondary GBE Ethernet interfaces is available on AFB pins as defined by SMARC specifications.
The following table describes secondary GBE signals organization.

PIN	NAME	PHY PIN NAME	NOTE
S18	GBE1_MDI0-	ETH2_TXRXM_A	Diff100
S17	GBE1_MDI0+	ETH2_TXRXP_A	
S21	GBE1_MDI1-	ETH2_TXRXM_B	Diff100
S20	GBE1_MDI1+	ETH2_TXRXP_B	
S23	GBE1_MDI2-	ETH2_TXRXM_C	Diff100
S24	GBE1_MDI2+	ETH2_TXRXP_C	
S27	GBE1_MDI3-	ETH2_TXRXM_D	Diff100
S26	GBE1_MDI3+	ETH2_TXRXP_D	
S19	GBE1_LINK100#	ETH2_nLINK	Output OD (12mA)
S22	GBE1_LINK1000#	+3V3 PU	Output OD (12mA)
S21	GBE1_LINK_ACT#	Link_n ACT	Output OD (12mA)

GBE_LINKx signal can be useful to drive Ethernet led indicators. Each output can drive up to 12 mA.
GBE_LINK100# Signal link for 10/100 Mb speed (**3,3V** Signal)
GBE_LINK_ACT# Signal act for any speed (**3,3V** Signal)
GBE_LINK1000# is GPIO controlled by the software (**3,3V** Signal)

The LED output signals GBE_LINK_ACT#, GBE_LINK100# and GBE_LINK1000# can be connected directly to the LED of the Ethernet jack with suitable serial resistors. There is no need for additional buffering if the current draw does not exceed 10mA. All GBE_LINKx signals act as link and activity indicators. The following table describes GBE_LINKx signal functionality.\\\

SIGNAL	NO LINK	10 Mb LINK/ACT	100 Mb LINK/ACT	1000 MB LINK/ACT
GBE_LINK100#	OFF	ON/BLINK	ON/BLINK	OFF

SIGNAL	NO LINK	10 Mb LINK/ACT	100 Mb LINK/ACT	1000 MB LINK/ACT
GBE_LINK1000#	OFF	ON/BLINK	OFF	ON/BLINK
GBE_LINK_ACT#	OFF	ON/BLINK	ON/BLINK	ON/BLINK

5.1.1 LAN Implementation Guidelines

The most critical component in the LAN interface is the isolation magnetics connected directly to the MDI differential pair signals of the SMARC module.

It should be carefully qualified for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection and Crosstalk Isolation to pass the IEEE conformance tests and EMI tests.

Even if a SMARC module complies with the basic specifications set forth for IEEE certification, it's still possible that the overall system could fail IEEE testing because of a poor quality or unsuitable external isolation magnetics module and/or improper PCB layout of the carrier board.

Ethernet connectors with integrated magnetics are preferable. If a design with external magnetics is chosen, additional care has to be taken to route the signals between the magnetics and Ethernet connector. If only Fast Ethernet (100Mbit/s) is required, some design cost may be saved by using only 10/100Base-TX magnetics.

The Ethernet MDI signals are analogue differential pair signals which need to be routed carefully.

Try to keep the MDI signals as short as possible and keep them away from digital signals. Try to avoid any stubs on these signals.

If discrete magnetics are used instead of a RJ-45 Ethernet jack with integrated magnetics, special care has to be taken to route the signals between the magnetics and the jack. These signals are required to be high voltage isolated from the other signals. It is therefore necessary to place a dedicated ground plane under these signals which has a minimum separation of 2mm from every other signal and plane.

The use of dedicated suppressor is recommended in order to avoid PHY damage by fast high transient voltage peak.

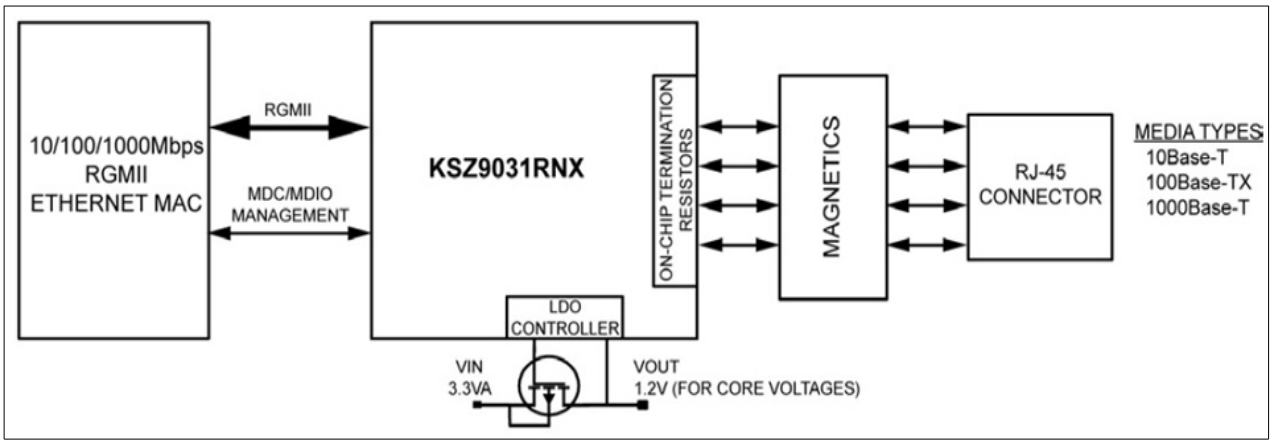
The PHY used in the module is the ***MICREL KSZ9031RNXIC***.

Refer to the ***MICREL Ethernet Physical Layer Layout Guidelines*** for more information.

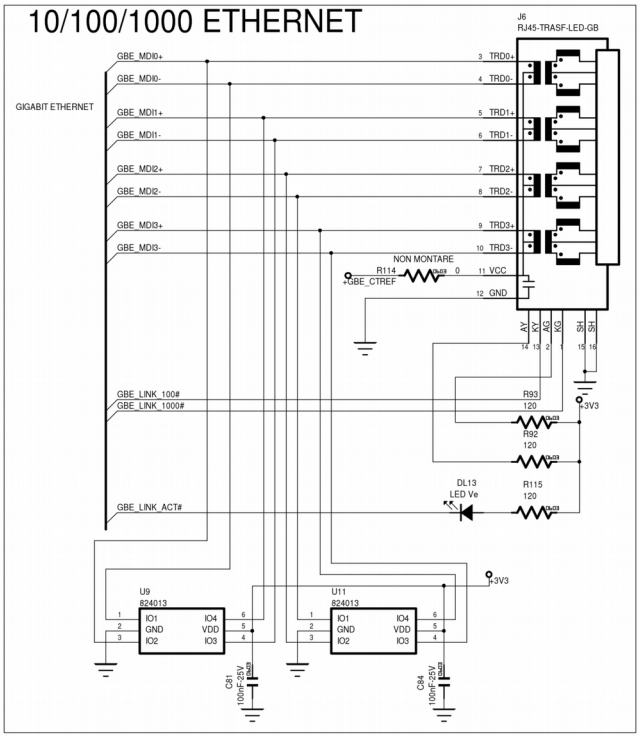
For a list of magnetics selected to operate with the MICREL KSZ9031RNXIC see KSZ9031RNX.pdf

The file is downloadable from the following link:

http://www.micrel.com/_PDF/Ethernet/datasheets/KSZ9031RNX.pdf



The need for centre tap voltage depends on the Ethernet PHY used on the SMARC module. In order to keep the carrier board compatible with all SMARC modules, the centre tap pins of the magnetics should all be connected to the centre tap voltage source pin of the module connector (GBE_CTREF).



The following figure shows a typical GBE connection.

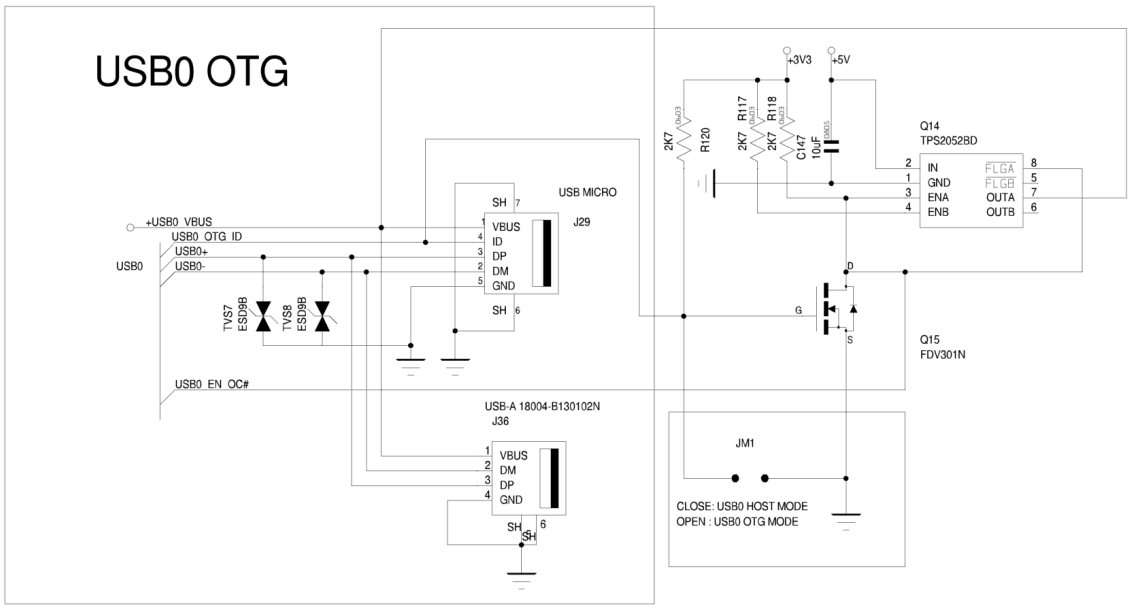
Note: refer to the Gbit Ethernet specifications for further details about the board's design and the relative PCB master.

5.2 USB

The USB0 port is available as a USB 2.0 and it may also be configured as an OTG or as a HOST port, these option are selected on the Engicam's carrier board by a jumper.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	NOTE
P60	USB0+	USB_OTG1_DP	N	USB	Diff90
P61	USB0-	USB_OTG1_DN	N	USB	
P62	USB0_EN_OC#	SAI1_TXD6/ SAI1_TXD7	Y	3.3V	10K PU on Module Enable signal for the bus voltage output and over current input signal for the USB0 interface Pulled low by module OD turns on power switch Pulled low by Carrier OD driver to indicate over-current situation occur
P63	USB0_VBUS_DET	USB0_VBUS	-	5V	To be controlled by software (5V tolerant)
P64	USB0_OTG_ID	USB1_ID	N	3.3V	

In the following image is shown the USB0 interface implementation on the carrier board



Also, the USB1 port is available as a USB 2.0 client. It is available as a host port, this is implemented on the Engicam's carrier board using a hub.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	NOTE
P65	USB1+	SM_USB1_DP	No	USB	Diff90
P66	USB1-	SM_USB1_DN	No	USB	
P67	USB1_EN_OC#	SM_USB1_EN_OC#	Yes	3.3V	10K PU on Module Enable signal for the bus voltage output and over current input signal for the USB1 interface Pulled low by module OD turns on power switch Pulled low by Carrier OD driver to indicate over-current situation occur

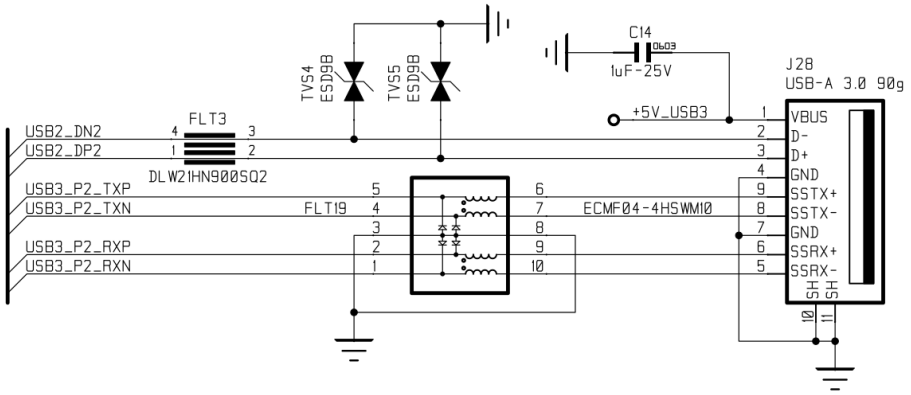
PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	NOTE
P69	USB2+	SM_USB2_DP	No	USB	Diff90
P70	USB2-	SM_USB2_DN	No	USB	Diff90
P71	USB2_EN_OC#	SM_USB2_EN_OC#	Yes	3.3V	10K PU on Module Enable signal for the bus voltage output and over current input signal for the USB1 interface Pulled low by module OD turns on power switch Pulled low by Carrier OD driver to indicate over-current situation occur

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	NOTE
S68	USB3+	SM_USB3_DP	No	USB	Diff90
S69	USB3-	SM_USB3_DN	No	USB	Diff90
P74	USB3_EN_OC#	SM_USB3_EN_OC#	Yes	+3.3V	3K3 PU on Module Enable signal for the bus voltage output and over current input signal for the USB3 interface. Pulled high by module. Carrier can pull low to disable USB. OC connected to USB2_OC1_N_1V8 on CPU.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	NOTE
S35	USB4+	SM_USB4_DP	No	USB	
S36	USB4-	SM_USB4_DN	No	USB	
P76	USB4_EN_OC#	SM_USB4_EN_OC#	Yes	+3.3V	3K3 PU on Module Enable signal for the bus voltage output and over current input signal for the USB3 interface. Pulled high by module. Carrier can pull low to disable USB. OC connected to USB2_OC1_N_1V8 on CPU.

USB 3.0

USB 3.0 interfaces have to be coupled with relative USB 2.0 interfaces. Figure below shows how to couple the interfaces on a standard USB 3.0 type A connector.



PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	NOTE
S72	USB2_SSTX-	USB2_TX_N	N	USB SS	To be coupled with USB2, pin P69 and P70.
S71	USB2_SSTX+	USB2_TX_P	N	USB SS	
S75	USB2_SSRX-	USB2_RX_N	N	USB SS	
S74	USB2_SSRX+	USB2_RX_P	N	USB SS	

5.3 HDMI

SMARC MX8M Plusw supports HDMI Interface.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
P92	HDMI_D2+ / DP1_LANE0+	HDMI_TXP2	N		Output	
P93	HDMI_D2- / DP1_LANE0-	HDMI_TXN2	N		Output	
P95	HDMI_D1+ / DP1_LANE1+	HDMI_TXP1	N		Output	
P96	HDMI_D1- / DP1_LANE1-	HDMI_TXN1	N		Output	
P98	HDMI_D0+ / DP1_LANE2+	HDMI_TXP0	N		Output	
P99	HDMI_D0- / DP1_LANE2-	HDMI_TXN0	N		Output	
P101	HDMI_CK+ / DP1_LANE3+	HDMI_CLKP	N		Output	
P102	HDMI_CK- / DP1_LANE3-	HDMI_CLKN	N		Output	
P104	HDMI_HPD / DP1_HPD	HDMI_HPD			Input	
P105	HDMI_CTRL_CK / DP1_AUX+	HDMI_DDC_SCL	Y		Output	
P106	HDMI_CTRL_DAT / DP1_AUX-	HDMI_DDC_SDA	Y		Output	

5.4 LVDS

In the SMACORE module there are 2 connection to display with LVDS interface up to Full HD resolution, the connection is up to 24 bit data.

Following the LVDS interfaces maps and schemes

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
S108	LVDS1_CK+	LVDS1_CLK_P	N	+2.5V	Output	
S109	LVDS1_CK-	LVDS1_CLK_N	N	+2.5V	Output	
S111	LVDS1_0+	LVDS1_DATA0_P	N	+2.5V	Output	
S112	LVDS1_0-	LVDS1_DATA0_N	N	+2.5V	Output	
S114	LVDS1_1+	LVDS1_DATA1_P	N	+2.5V	Output	
S115	LVDS1_1-	LVDS1_DATA1_N	N	+2.5V	Output	
S117	LVDS1_2+	LVDS1_DATA2_P	N	+2.5V	Output	
S118	LVDS1_2-	LVDS1_DATA2_N	N	+2.5V	Output	
S120	LVDS1_3+	LVDS1_DATA3_P	N	+2.5V	Output	
S121	LVDS1_3-	LVDS1_DATA3_N	N	+2.5V	Output	
S107	LVDS1_BKLT_EN	GPIO3_IO28	Y	+3,3V	Output	
S141	LCD BKLT_PWM	PWM2_OUT	Y	+3,3V	Output	
S125	LVDS0_0+	LVDS0_DATA0_P	N	+2.5V	Output	
S126	LVDS0_0-	LVDS0_DATA0_N	N	+2.5V	Output	
S128	LVDS0_1+	LVDS0_DATA1_P	N	+2.5V	Output	
S129	LVDS0_1-	LVDS0_DATA1_N	N	+2.5V	Output	
S131	LVDS0_2+	LVDS0_DATA2_P	N	+2.5V	Output	
S132	LVDS0_2-	LVDS0_DATA2_N	N	+2.5V	Output	
S134	LVDS0_CK+	LVDS0_CLK_P	N	+2.5V	Output	
S135	LVDS0_CK-	LVDS0_CLK_N	N	+2.5V	Output	
S137	LVDS0_3+	LVDS0_DATA3_P	N	+2.5V	Output	
S138	LVDS0_3-	LVDS0_DATA3_N	N	+2.5V	Output	

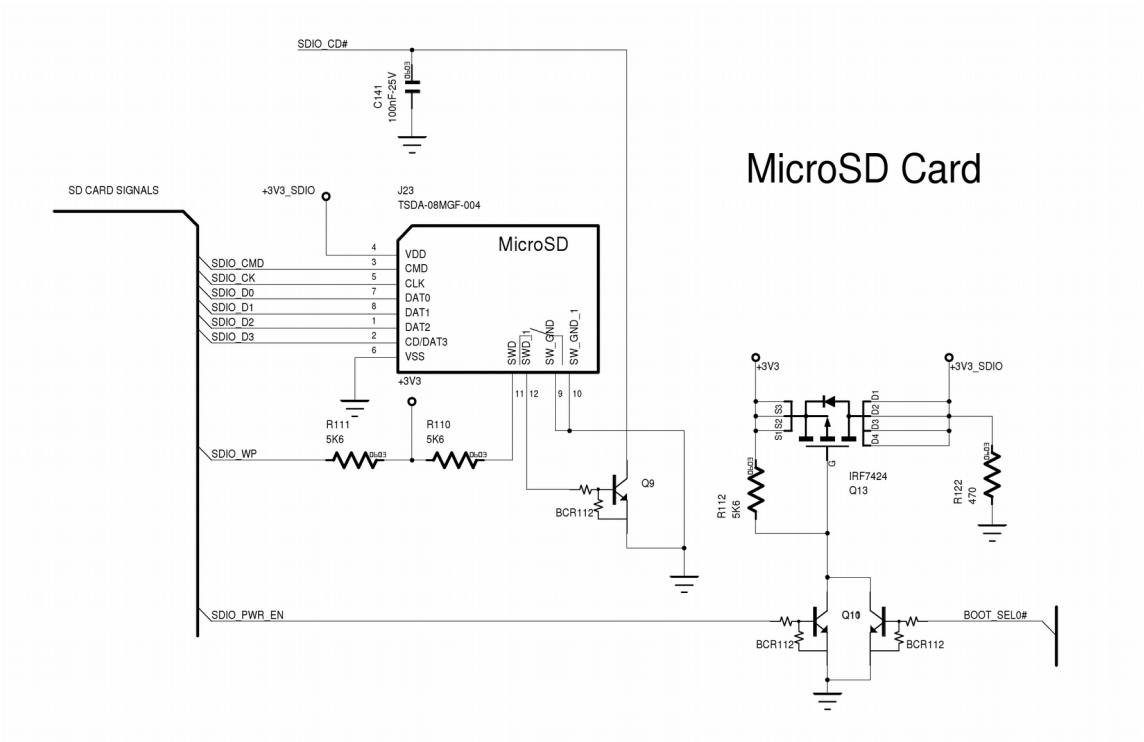
5.4.1 LVDS Routing and Placement Considerations

The LVDS lines are high-speed signals and as such during the designing must be complied with standards of protection against noise and crosstalk. In this chapter we give some advices about positioning, cabling and routing; for further details, follow the guidelines and the manuals about LVDS bus.
Differential line: as mentioned we are working with fast signals, then to avoid disturbances and reduce noise on the line we suggest routing the channel lines in differential mode, for the same reason also the “channel” on the cable used to connect the board to TFT should be twisted.
Distance: there is no distance recommended between the devices but, always considering the nature of signals and that the driver is the same processor i.MX6SX, we suggest to positioning the connector as close as possible to the module, and also to be aware to matching the line of differential pair as best as you can to avoid any kind of delay.
Controlled Impedance: all the signal's pairs must be traced in controlled impedance referred to the GND plane. This should avoid the problems due to reflections on the line. We suggest that the traces for LVDS signals should be closely-coupled and designed for 100Ω differential impedance.

5.5 SDIO

The module implements SDIO Interface including cards with reduced size or mini cards. The figure below shows how the Micro SD Card connector is connected to the Module in the evaluation board. The SDIO signals of the module's main connector are listed in table below.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
P33	SDIO_WP	SD2_WP	Y	3,3V	Input	Write protect
P34	SDIO_CMD	SD2_CMD	Y	3,3V	Bi-Dir	Command line
P35	SDIO_CD#	SD2_CD_B	Y	3,3V	Input	Card Detect
P36	SDIO_CK	SD2_CLK	Y	3,3V	Output	Clock
P37	SDIO_PWR_EN	SD2_RESET_B	Y	3,3V	Output	SD power enable
P39	SDIO_D0	SD2_DATA0	Y	3,3V	Bi-Dir	Data
P40	SDIO_D1	SD2_DATA1	Y	3,3V	Bi-Dir	Data
P41	SDIO_D2	SD2_DATA2	Y	3,3V	Bi-Dir	Data
P42	SDIO_D3	SD2_DATA3	Y	3,3V	Bi-Dir	Data



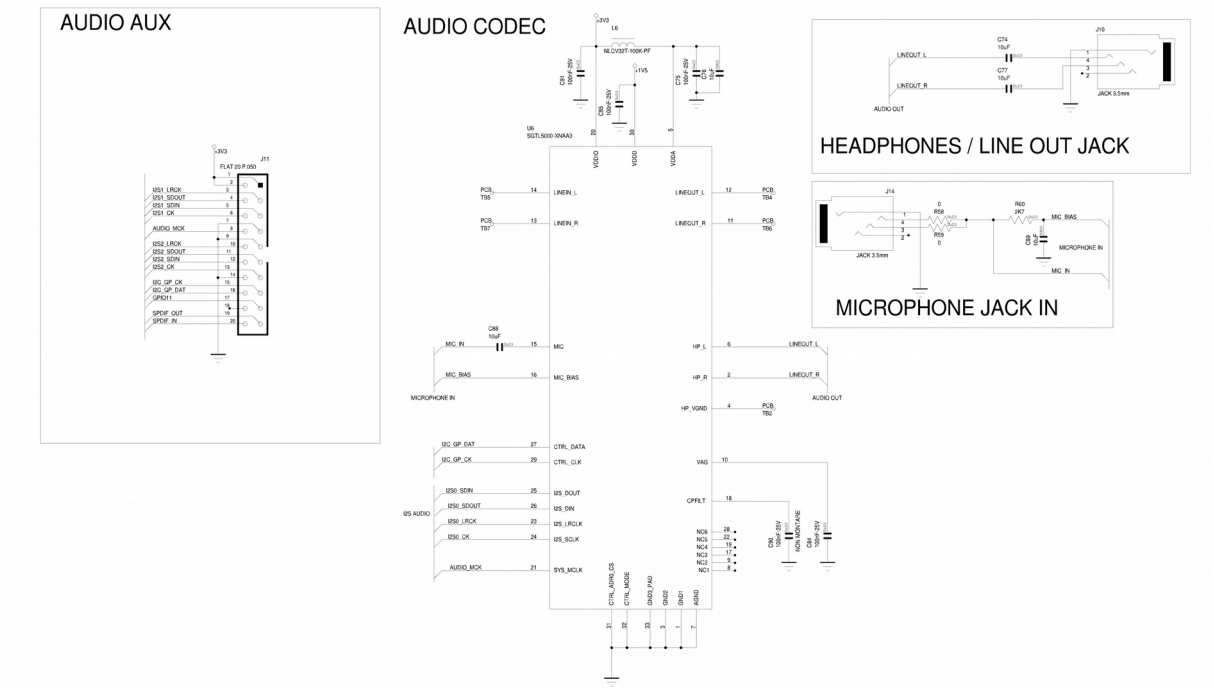
The Module pin definition allows for an 8 bit eMMC interface. The eMMC (embedded Multi Media Card) interface, used to connect non-volatile multimedia memory devices to host processor, is implemented using an “expansion” interface connector.

5.6 I2S

I2S, (**Integrated Interchip Sound)**, or **IIS**, is an electrical serial bus interface standard used for connecting digital audio devices.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
S38	AUDIO_MCK	SAI3_MCLK	-	CMOS VDD_IO	Output	Master clock output to Audio codecs
S39	I2S0_LRCK	SAI3_TXFS	Y	CMOS VDD_IO	Bi-Dir	Left-Right audio sync clock
S40	I2S0_SDOUT	SAI3_TXD	Y	CMOS VDD_IO	Output	Digital audio Output
S41	I2S0_SDIN	SAI3_RXD	Y	CMOS VDD_IO	Input	Digital audio Input
S42	I2S0_CK	SAI3_TXC	Y	CMOS VDD_IO	Bi-Dir	Digital audio clock

The I2S bus may have a single bidirectional data line or two separate data lines. The bus consists of at least three lines: a serial clock/ bit clock (output from the master), a left right clock (output from the master) that indicates the channel being transmitted and a single data line. It may also include a second data line – and a Master clock signal. A SMARC module can generally be configured as I2S master or slave.
The Engicam's SMARC modules may support up to two independent I2S interfaces both having separate input and output data lines.



5.7 SPI

In the SMARC modules is available two SPI interfaces, as the SMARC's standard required.
The following tables describe the Enhanced Configurable SPI signals

SPI0

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
P43	SPI0_CS0#	ECSPI1_SS0	Y	CMOS VDD_IO	Output	
P44	SPI0_CK	ECSPI1_SCLK	Y	CMOS VDD_IO	Output	
P45	SPI0_DIN	ECSPI1_MISO	Y	CMOS VDD_IO	Input	
P46	SPI0_DO	ECSPI1_MOSI	Y	CMOS VDD_IO	Output	

ECSPI

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
P54	ESPI_CS0#	NAND_CE0_B	Y	CMOS VDD_IO	Output	
P55	ESPI_CS1#	NAND_CE0_B	Y	CMOS VDD_IO	Output	
P56	ESPI_CK	NAND_ALE	Y	CMOS VDD_IO	Output	
P58	ESPI_IO_0	NAND_DATA00	Y	CMOS VDD_IO	Input	
P57	ESPI_IO_1	NAND_DATA01	Y	CMOS VDD_IO	Output	
S56	ESPI_IO_2	NAND_DATA02	Y	CMOS VDD_IO	Output	
S57	ESPI_IO_3	NAND_DATA03	Y	CMOS VDD_IO	Output	

5.8 SERIALS

As required into the SMARC specifications the module has up to four asynchronous serial ports interfaces labelled SER 0 – SER3.

The signal on the module's UART pins are 3.3V logic level, this cannot be connected directly to a RS232 device like a PC Serial port, the use of a transceivers on the base board is mandatory in order to avoid module damage.

The following tables describe the specifications of the 4 wires interfaces

SER0

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
P129	SER0_TX	UART2_TXD	Y	CMOS VDD_IO	Output	
P130	SER0_RX	UART2_RXD	Y	CMOS VDD_IO	Input	
P131	SER0_RTS#	SD1_DATA5	Y	CMOS VDD_IO	Output	Shared signal
P132	SER0_CTS#	SD1_DATA4	Y	CMOS VDD_IO	Input	Shared signal

SER1

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
P134	SER1_TX	UART1_TXD	Y	CMOS VDD_IO	Output	
P135	SER1_RX	UART1_RXD	Y	CMOS VDD_IO	Input	

SER2

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
P136	SER2_TX	SD1_DATA6	Y	CMOS VDD_IO	Output	
P137	SER2_RX	SD1_DATA7	Y	CMOS VDD_IO	Input	
P138	SER2_RTS#	SD1_STROBE	Y	CMOS VDD_IO	Output	Shared signal
P139	SER2_CTS#	SD1_RESET	Y	CMOS VDD_IO	Input	Shared signal

SER3

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
P140	SER3_TX	UART4_TXD	Y	CMOS VDD_IO	Output	
P141	SER3_RX	UART4_RXD	Y	CMOS VDD_IO	Input	

Note: *the SER0' is used as Linux Console*

5.9 CAN

Following is described the two CAN bus interfaces available on the module (the specification defines both CAN interfaces as optional)

CAN0

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
P143	CAN0_TX	SPDIF_TX	Y	CMOS VDD_IO	Output	
P144	CAN0_RX	SPDIF_RX	Y	CMOS VDD_IO	Input	

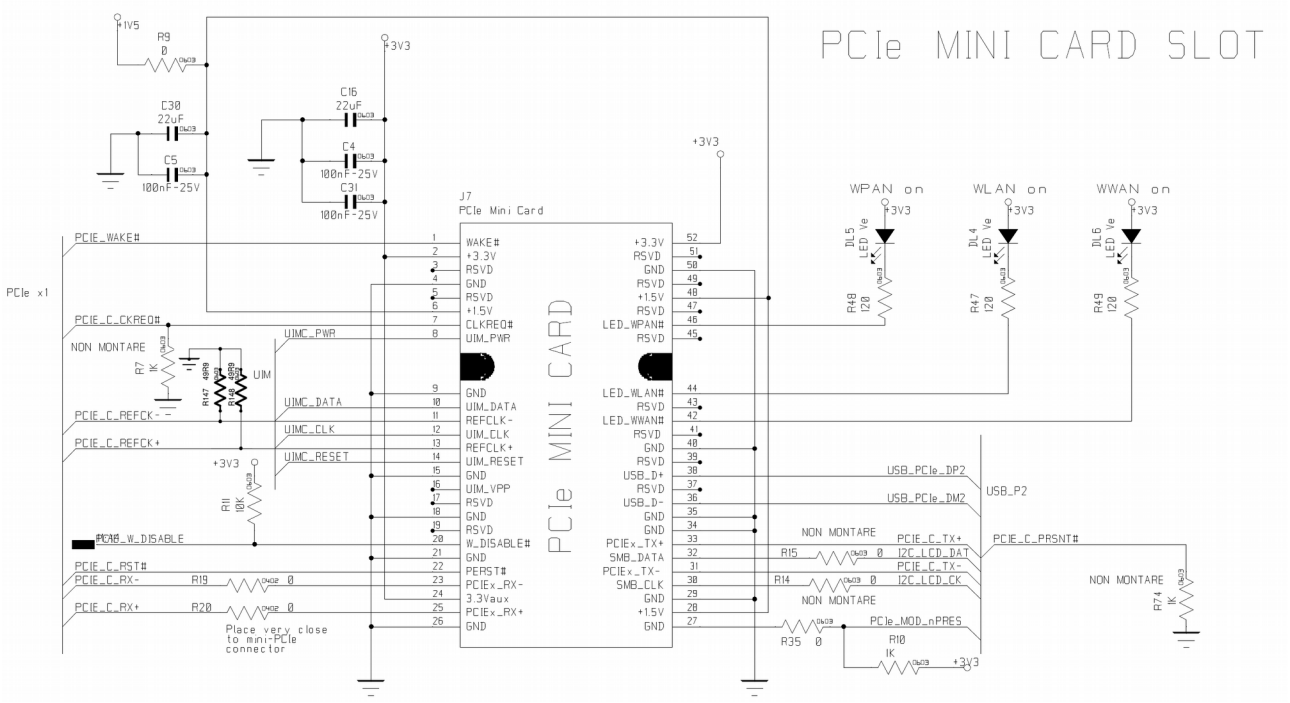
CAN1

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
P145	CAN1_TX	UART3_RXD	Y	CMOS VDD_IO	Output	
P146	CAN1_RX	UART3_TXD	Y	CMOS VDD_IO	Input	

5.10 PCIe

Compliant with the specification the module implements the PCIe Link A port

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
P75	PCIE_A_RST#	SAI5_RXD2	Y	3,3V	Output	PCIe reset
P83	PCIE_A_REFCK+	PCIE1_REF_CLKIN_P	N	CMOS VDD_IO	Output	Differential PCIe reference clock
P84	PCIE_A_REFCK-	PCIE1_REF_CLKIN_N	N	CMOS VDD_IO	Output	Differential PCIe reference clock
P86	PCIE_A_RX+	PCIE_RX_P	N	CMOS VDD_IO	Input	Differential PCIe receive data
P87	PCIE_A_RX-	PCIE_RX_N	N	CMOS VDD_IO	Input	Differential PCIe receive data
P89	PCIE_A_TX+	PCIE_TX_P	N	CMOS VDD_IO	Output	Differential PCIe transmit data
P90	PCIE_A_TX-	PCIE_TX_N	N	CMOS VDD_IO	Output	Differential PCIe transmit data
S146	PCIE_WAKE#	SPDIF_EXT_CLK	Y	3,3V	Input	PCIe wake up interrupt



Termination is required on the differential clock lines. Connect two 49.9 Ω resistors, one between REFCLK and GND, the other between REFCLK+ and GND. Alternately, Connect a 100 Ω resistor between REFCLK- and REFCLK+, as close as possible to the receiver device (connector).

Note: for further details, refer to PCIe recommendations on iMx6 series document (as design guide IMX6SXHDG and reference manual).

5.11 GPIO

The following pins, compliant with SMARC specifications, are allocated as general purpose IO, they have all the bidirectional capability but also a preferred direction.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
P108	GPIO0/CAM0_PWR#	GPIO1_IO00	Y	CMOS VDD_IO	Input / Output	
P109	GPIO1/CAM1_PWR#	GPIO1_IO04	Y	CMOS VDD_IO	Input / Output	
P110	GPIO2/CAM0_RST#	GPIO1_IO05	Y	CMOS VDD_IO	Input / Output	
P111	GPIO3/CAM1_RST#	GPIO1_IO07	Y	CMOS VDD_IO	Input / Output	
P112	GPIO4/HDA_RST#	GPIO1_IO08	Y	CMOS VDD_IO	Input / Output	
P113	GPIO5/PWM_OUT	GPIO1_IO15	Y	CMOS VDD_IO	Input / Output	
P114	GPIO6/TACHIN	GPIO1_IO09	Y	CMOS VDD_IO	Input / Output	
P115	GPIO7/PCAM_FLD	GPIO1_IO10	Y	CMOS VDD_IO	Input / Output	
P116	GPIO8/CAN0_ERR#	GPIO1_IO12	Y	CMOS VDD_IO	Input / Output	
P117	GPIO9/CAN1_ERR#	GPIO1_IO13	Y	CMOS VDD_IO	Input / Output	
P118	GPIO10	GPIO1_IO14	Y	CMOS VDD_IO	Input / Output	
P119	GPIO11	SAI2_RXFS	Y	CMOS VDD_IO	Input / Output	

5.12 Camera Interface

The following pin are implemented to support Camera interface using the CMOS sensor interface of the module

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
P3	CSI1_CK+	MIPI_CSI1_CLK_P	Y	CMOS VDD_IO	Input	Parallel camera input data
P4	CSI1_CK-	MIPI_CSI1_CLK_N	Y	CMOS VDD_IO	Input	Parallel camera input data
P7	CSI1_RX0+	MIPI_CSI1_D0_P	Y	CMOS VDD_IO	Input	Parallel camera input data
P8	CSI1_RX0-	MIPI_CSI1_D0_N	Y	CMOS VDD_IO	Input	Parallel camera input data
P10	CSI1_RX1+	MIPI_CSI1_D1_P	Y	CMOS VDD_IO	Input	Parallel camera input data
P11	CSI1_RX1-	MIPI_CSI1_D1_N	Y	CMOS VDD_IO	Input	Parallel camera input data
P13	CSI1_RX2+	MIPI_CSI1_D2_P	Y	CMOS VDD_IO	Input	Parallel camera input data
P14	CSI1_RX2-	MIPI_CSI1_D2_N	Y	CMOS VDD_IO	Input	Parallel camera input data
P16	CSI1_RX3+	MIPI_CSI1_D3_P	Y	CMOS VDD_IO	Input	Parallel camera input data
P17	CSI1_RX3-	MIPI_CSI1_D3_N	Y	CMOS VDD_IO	Input	Parallel camera input data
S1	CSI1_TX+/ I2C_CAM1_CK	SAI5_RXD0		CMOS VDD_IO	Output	Parallel camera output
S2	CSI1_TX-/ I2C_CAM1_DAT	SAI5_MCLK	Y	CMOS VDD_IO	Output	Parallel camera output

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
S8	CSI0_CK+	MIPI_CSI1_CLK_P	Y	CMOS VDD_IO	Input	Parallel camera input data
S9	CSI0_CK-	MIPI_CSI1_CLK_N	Y	CMOS VDD_IO	Input	Parallel camera input data
S11	CSI0_RX0+	MIPI_CSI1_D0_P	Y	CMOS VDD_IO	Input	Parallel camera input data
S12	CSI0_RX0-	MIPI_CSI1_D0_N	Y	CMOS VDD_IO	Input	Parallel camera input data
S14	CSI0_RX1+	MIPI_CSI1_D1_P	Y	CMOS VDD_IO	Input	Parallel camera input data
S15	CSI0_RX1-	MIPI_CSI1_D1_N	Y	CMOS VDD_IO	Input	Parallel camera input data

The I2C_CAM port is intended to support serial and parallel cameras (SMARC specification).
The module implements the I2C_CAM on I2C2 interface on module

5.13 PWM

It's possible to set the pins shown in the following table as PWM output signals.

PIN	NAME PWM1_OUT	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
p113	GPIO1_IO15	GPIO1_IO15	Y	CMOS VDD_IO	Output	PWM4_OUT
S141	PWM2_OUT	GPIO1_IO11	Y	CMOS VDD_IO	Output	PWM2_OUT
S142	GPIO12	GPIO1_IO01	Y	CMOS VDD_IO	Output	PWM1_OUT

5.14 I2C

An I2C interface is needed for MOST bus support. The Module I2C_GP port may be used.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
S1	CSI1_TX+/I2C_CAM1_CK	SAI5_RXD0	Y	CMOS VDD_IO	Input	Parallel camera output
S2	CSI1_TX-/I2C_CAM1_DAT	SAI5_MCLK	Y	CMOS VDD_IO	Bi-Dir	Parallel camera output
S5	CSI0_TX+/I2C_CAM0_CK	I2C3_SCL	Y	CMOS VDD_IO	Input	Parallel camera output
S7	CSI0_TX-/I2C_CAM0_DAT	I2C3_SDA	Y	CMOS VDD_IO	Bi-Dir	Parallel camera output
S48	I2C_GP_CK	I2C2_SCL	Y	CMOS VDD_IO	Input	I2C Bus Clock
S49	I2C_GP_DAT	I2C2_SDA	Y	CMOS VDD_IO	Bi-Dir	I2C Bus Data
P105	HDMI_CTRL_CK	HDMI_DDC_SCL	Y	CMOS VDD_IO	Input	I2C Bus Clock
P106	HDMI_CTRL_DAT	HDMI_DDC_SDA	Y	CMOS VDD_IO	Bi-Dir	I2C Bus Data
P121	I2C_PM_CK	SAI5_RXFS	Y	CMOS VDD_IO	Input	I2C Bus Clock
P122	I2C_PM_DAT	SAI5_RXC	Y	CMOS VDD_IO	Bi-Dir	I2C Bus Data
S139	I2C_LCD_CK	I2C4_SCL	Y	CMOS VDD_IO	Input	I2C Bus Clock
S140	I2C_LCD_DAT	I2C4_SDA	Y	CMOS VDD_IO	Bi-Dir	I2C Bus Data

One I2C-bus slave address (1101000R/W)) is reserved for the PCF8523 on I2C6 (P121, P122)
One I2C-bus slave address (1001000R/W) is reserved for the SE050 (if present) on I2C4