i.Core MX8MP HW Manual Preliminary
Getting started manual

Revision History

DATE	REVISION	CHANGE DESCRIPTION
dd/mm/2020	1.0.0	Release

Table of Contents

Chapter

1

1. Introduction

This Chapter gives background information on this document.

Section includes:

- ✔ **General Overview**
- ✔ **Acronyms and Abbreviations Used**
- ✔ **Document and Standard References**

1.1 General Information

This document is created to guide users to design i.MX8MP compliant carrier boards. It will focus only on the interfaces in i.MX8MP pinouts and related peripherals.

This document helps walk hardware designers through the various stages of designing a carrier board on this platform. Using this document, hardware designers can efficiently locate the resources they need at every step in the board design flow.

All examples of this document are based on carrier board that is available from ENGICAM. This document also provides a collection of useful documentation, application reports, and design recommendations.

1.2 Block Diagram

1.3 Main Features

1.4 Document and Standard References

1.4.1 External Industry Standard Documents

- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com).
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com).
- USB Specifications (www.usb.org).

1.4.2 Other external documents

i.MX8MP Hardware Developer's Guide

iMX8MPi_RM

IMX8MPCEC

1.4.3 On-line documentation

1.5 Disclaimer

Information in this document is provided solely to enable system and software implementers to use Engicam products. Engicam does not guarantee that the information in this manual is up-to-date, correct, complete or of good quality. Nor does Engicam assume guarantee for further usage of the information.

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Engicam explicitly reserves the rights to change or add to the contents of this manual or parts of it without special notification. All operating parameters must be validated for each customer application by customer's technical experts.

1.6 Support

We offer on-line support to allow the customer to stay updated on the development of software release and on the enhancement of the documentation.

Following is shown the references for ENGICAM on-line support.

www.engicam.com

ENGICAM Product Experts are available to answer questions via email:

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1.7 Acronyms and Abbreviations used

ABBREVIATION	EXPLANATION
ADC	Analogue to Digital Converter
CAN	Controller Area Network, a bus that is manly used in automotive and industrial environment
CPU	Central Processor Unit
DAC	Digital to Analogue Converter
EMI	Electromagnetic Interference, high frequency disturbances
eMMC	Embedded Multi Media Card, flash memory combined with MMC interface controller in a BGA package, used as internal flash memory
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
GND	Ground
GPIO	General Purpose Input/Output, pin that can be configured being an input or output
HDMI	High-Definition Multimedia Interface, combines audio and video signal
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PD	Pull Down Resistor
PHY	Physical Layer of the OSI model
PMIC	Power Management IC, integrated circuit that manages amongst others the power sequence of a system
PU	Pull Up Resistor
PWM	Pulse-Width Modulation
RGB	Red Green Blue, colour channels in common display interfaces
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SPI	Serial Peripheral Interface Bus, synchronous four wire full duplex bus for peripherals
USB	Universal Serial Bus, serial interface for internal and external peripherals

Chapter

2

2. Mechanical data

This Chapter gives information about PCB and module's dimensions.

Section includes:

- ✔ **Assembly Top View**
- ✔ **Assembly Bottom View**
- ✔ **Mechanical data**

2.1 Mechanical data

The iMX8MP module has a standard SO DIMM footprint compliant with TYCO ELECTRONICS code 1473005-1 or compatible connector. The PCB dimensions is L 67.60 x W 32.1 x H 1 mm. The distances available on PCB under the module are from **1** to 1,4 mm

2.2 Assembly Top View

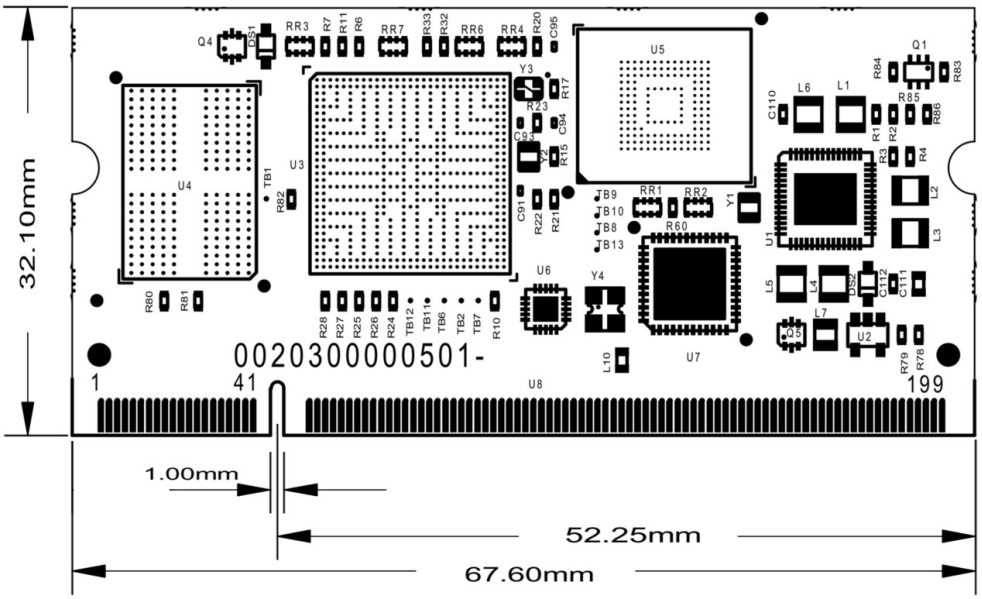


Figure 1

2.3 Assembly Bottom View

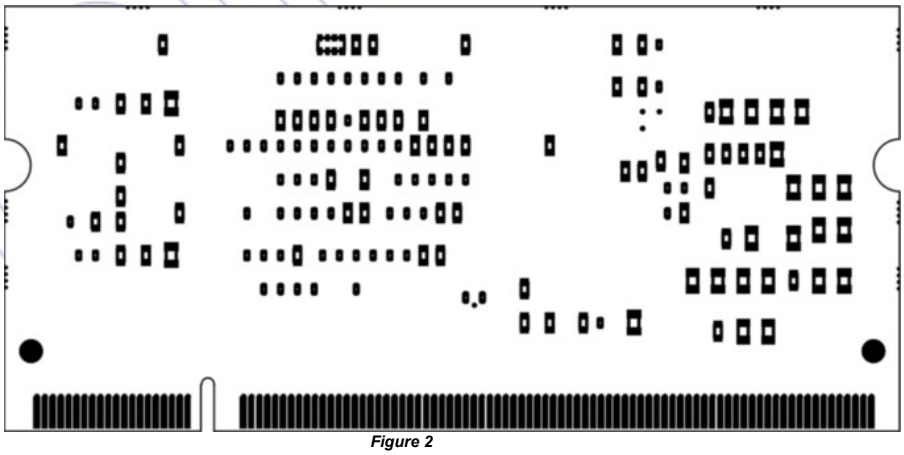


Figure 2

Chapter

3

3. Ordering Information and Features

This Chapter gives the ordering information and technical specifications of the modules.

Section includes:

- ✔ **i.CoreMX8MP ordering codes**
- ✔ **CPU & Memory specification**
- ✔ **Operating temperature range**
- ✔ **i.MX8MP supported features**

3.1 Ordering Information

Following is provided the ordering information and the description for the Basic technical specifications modules:

Marking Code	Ordering Code	MPQ	Description	CPU & Memory specifications	Operating temperature range °C (excepted CPU)	Module available at least until [1]
i.Core MX8MP	tbd	1			-25 to +85	4thQ -2030
i.Core MX8MP	tbd	58			-25 to +85	4thQ -2030
i.Core MX8MP	tbd	1			-25 to +85	4thQ -2030
i.Core MX8MP	tbd	58			-25 to +85	4thQ -2030

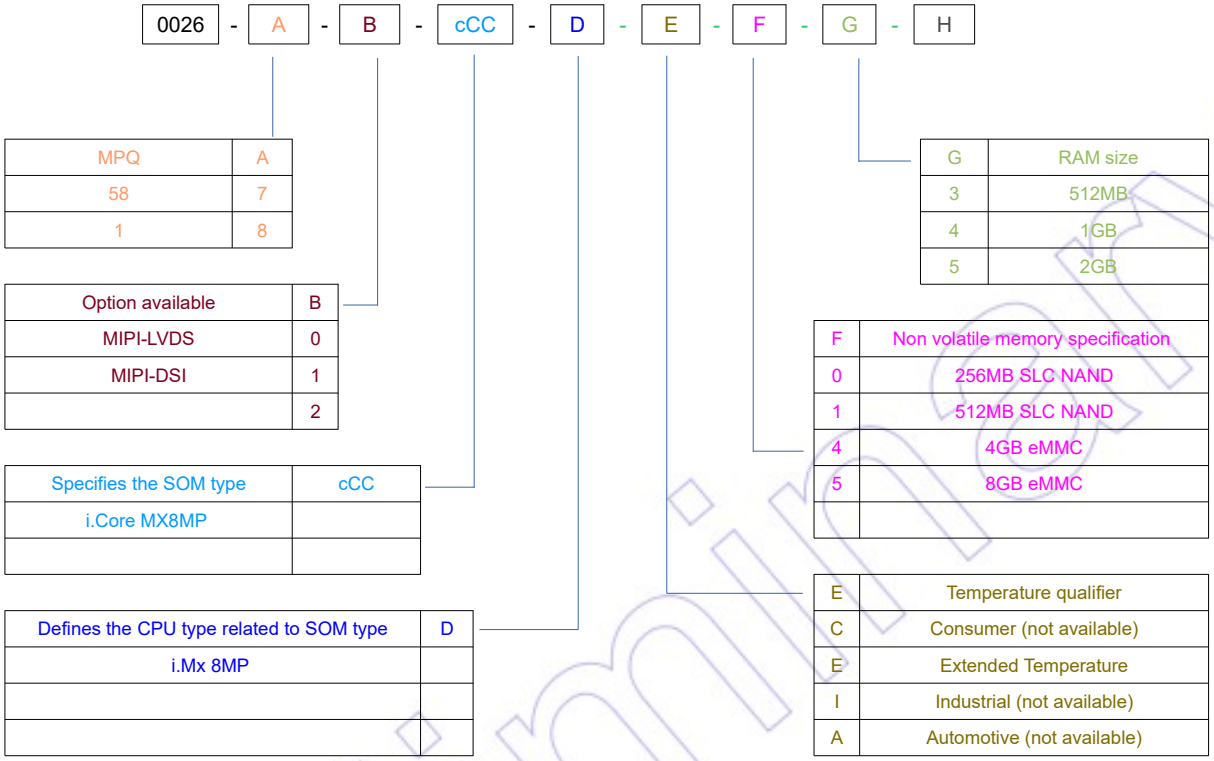
Table 1

[1] *Long Term Availability based on NXP longevity program*
[2] *Note: internal junction temperature (for further information see NXP documentation)*

WARNING: the actual temperature depend on the application, the enclosure and/or the environmental condition. Upon customer to consider specific cooling solutions for its own final system.

3.2 Part Number Structure

The module is available with eMMC option. *The standard order codes shown in the tables above shall be modified as follow:*



WARNING: not all the custom configurations might be available in respect of standard times and orderable quantities

Chapter

4

4. Pinout and Electrical Specifications

This Chapter gives the pinout information.

Section includes:

- ✔ **Pinout overview**
- ✔ **Pad specifications**
- ✔ **Electrical specifications**

4.1 Module Pinout

The module's interface is achieved by a SO DIMM 200 position connector TYCO ELECTRONICS code 1473005-1 or compatible

Pin	Name	Pin Name on I.MX8MP	Primary Function Description	GPIO Capable	Voltage
1	+1V8	-	Output Power PIN	-	-
2	+1V8	-	Output Power PIN	-	-
3	GND	-	Power PIN	N	-
4	GND	-	Power PIN	N	-
5	GND	-	Power PIN	N	-
6	GPIO1_IO00	GPIO1_IO00	Generic GPIO	Y	+3,3V
7	GPIO4_IO09	SAI1_RXD7	Generic GPIO	Y	+3,3V
8	GPIO1_IO03	GPIO1_IO03	Generic GPIO	Y	+3,3V
9	GPIO1_IO04	GPIO1_IO04	Generic GPIO	Y	+3,3V
10	GPIO1_IO05	GPIO1_IO05	Generic GPIO	Y	+3,3V
11	GPIO1_IO06	GPIO1_IO06	Generic GPIO	Y	+3,3V
12	GPIO1_IO07	GPIO1_IO07	Generic GPIO	Y	+3,3V
13	GPIO1_IO08	GPIO1_IO08	Generic GPIO	Y	+3,3V
14	GPIO1_IO09	GPIO1_IO09	Generic GPIO	Y	+3,3V
15	GPIO1_IO10	GPIO1_IO10	Generic GPIO	Y	+3,3V
16	GPIO1_IO12	GPIO1_IO12	Generic GPIO	Y	+3,3V
17	GPIO1_IO13	GPIO1_IO13	Generic GPIO	Y	+3,3V
18	NC	-	-	-	-
19	HDMI_DDC_SCL	HDMI_DDC_SCL	HDMI I2C SCL Signal	-	+3,3V
20	HDMI_DDC_SDA	HDMI_DDC_SDA	HDMI I2C SDA Signal	-	+3,3V
21	+1,8V	-	JTAG ref Voltage	-	-
22	GND	-	Power PIN	N	-
23	I2C2_SCL	I2C2_SCL	I2C SCL Signal	Y	+3,3V
24	I2C2_SDA	I2C2_SDA	I2C SDA Signal	Y	+3,3V
25	GPIO1_IO14	GPIO1_IO14	Generic GPIO	Y	+3,3V
26	GPIO1_IO15	GPIO1_IO15	Generic GPIO	Y	+3,3V
27	ECSPI1_SS0	ECSPI1_SS0	SPI Interface	Y	+3,3V
28	ECSPI1_MOSI	ECSPI1_MOSI	SPI Interface	Y	+3,3V
29	ECSPI1_MISO	ECSPI1_MISO	SPI Interface	Y	+3,3V
30	ECSPI1_SCLK	ECSPI1_SCLK	SPI Interface	-	-
31	GND	-	Power PIN	N	-
32	GPIO5_IO03	SPDIF_TX	Generic GPIO	Y	+3,3V
33	GPIO5_IO04	SPDIF_RX	Generic GPIO	Y	+3,3V
34	SAI3_MCLK	SAI3_MCLK	Generic GPIO	Y	+3,3V
35	GPIO5_IO05	SPDIF_EXT_CLK	Generic GPIO	Y	+3,3V
36	GPIO2_IO09	SD1_DATA7	Generic GPIO	Y	+3,3V

Pin	Name	Pin Name on I.MX8MP	Primary Function Description	GPIO Capable	Voltage
37	GPIO4_IO21	SAI2_RXFS	Generic GPIO	Y	+3,3V
38	GPIO4_IO22	SAI2_RXC	Generic GPIO	Y	+3,3V
39	GND	-	Power PIN	-	-
40	SAI2_MCLK	SAI2_MCLK		Y	+3,3V
41	LVDS1_TX2_N	LVDS1_D2_N	LVDS Interface's Signals	N	+2,5V
42	LVDS0_TX3_P	LVDS0_D3_P	LVDS Interface's Signals	N	+2,5V
43	LVDS1_TX2_P	LVDS1_D2_P	LVDS Interface's Signals	N	+2,5V
44	LVDS0_TX3_N	LVDS0_D3_N	LVDS Interface's Signals	N	+2,5V
45	NC	-	-	-	-
46	LVDS0_CLK_P	LVDS0_CLK_P	LVDS Interface's Signals	N	+2,5V
47	LVDS1_TX3_N	LVDS1_D3_N	LVDS Interface's Signals	N	+2,5V
48	LVDS0_CLK_N	LVDS0_CLK_N	LVDS Interface's Signals	N	+2,5V
49	LVDS1_TX3_P	LVDS1_D3_P	LVDS Interface's Signals	N	+2,5V
50	LVDS0_TX1_P	LVDS0_D1_P	LVDS Interface's Signals	N	+2,5V
51	LVDS1_TX1_N	LVDS1_D1_N	LVDS Interface's Signals	N	+2,5V
52	LVDS0_TX1_N	LVDS0_D1_N	LVDS Interface's Signals	N	+2,5V
53	LVDS1_TX1_P	LVDS1_D1_P	LVDS Interface's Signals	N	+2,5V
54	LVDS1_TX0_N	LVDS1_D0_N	LVDS Interface's Signals	N	+2,5V
55	LVDS1_CLK_N	LVDS1_CLK_N	LVDS Interface's Signals	N	+2,5V
56	LVDS1_TX0_P	LVDS1_D0_P	LVDS Interface's Signals	N	+2,5V
57	LVDS1_CLK_P	LVDS1_CLK_P	LVDS Interface's Signals	N	+2,5V
58	LVDS0_TX2_P	LVDS0_D2_P	LVDS Interface's Signals	N	+2,5V
59	LVDS0_TX0_P	LVDS0_D0_P	LVDS Interface's Signals	N	+2,5V
60	LVDS0_TX2_N	LVDS0_D2_N	LVDS Interface's Signals	N	+2,5V
61	LVDS0_TX0_N	LVDS0_D0_N	LVDS Interface's Signals	N	+2,5V
62	SAI2_DIN	SAI2_RXD0		Y	+3,3V
63	SAI2_SCLK	SAI2_TXC		Y	+3,3V
64	GND	-	Power PIN	N	-
65	SAI2_LRCLK	SAI2_TXFS		Y	+3,3V
66	SAI2_DOUT	SAI2_TXD0		Y	+3,3V
67	PCIE_RX_N	PCIE_RXN_N	PCIe Interface	N	-
68	ECSPI2_SCLK	ECSPI2_SCLK	SPI Interface	Y	+3,3V
69	PCIE_RX_P	PCIE_RXN_P	PCIe Interface	N	-
70	HDMI_HPD	HDMI_HPD		Y	+3,3V
71	GND	-	Power PIN	N	-
72	PCIE_TX_N	PCIE_TXN_N	PCIe Interface	N	-
73	HDMI_CEC	HDMI_CEC		Y	+3,3V
74	PCIE_TX_P	PCIE_TXN_P	PCIe Interface	N	-
75	HDMI_CLKN	HDMI_TXC_N	-	N	-
76	PCIE_REF_CLK_N	PCIE_REF_PAD_CLK_N	PCIe Interface	N	-

Pin	Name	Pin Name on I.MX8MP	Primary Function Description	GPIO Capable	Voltage
77	HDMI_CLKP	HDMI_TXC_P	-	N	-
78	PCIE_REF_CLK_P	PCIE_REF_PAD_CLK_P	PCIe Interface	N	-
79	ECSPI2_MOSI	ECSPI2_MOSI	SPI Interface	Y	+3,3V
80	nSD_BOOT	-	External Interface Module	Y	+3,3V
81	HDMI_TXN0	HDMI_TX0_N	-	N	-
82	ECSPI2_MISO	ECSPI2_MISO	SPI Interface	Y	+3,3V
83	HDMI_TXP0	HDMI_TX0_P	-	N	-
84	ECSPI2_SS0	ECSPI2_SS0	SPI Interface	Y	+3,3V
85	HDMI_TXN1	HDMI_TX1_N	-	N	-
86	UART4_TXD	UART4_TXD	UART TX DATA signal	Y	+3,3V
87	HDMI_TXP1	HDMI_TX1_P	-	N	-
88	UART4_RXD	UART4_RXD	UART RX DATA signal	Y	+3,3V
89	GND	-	Power PIN	N	-
90	GPIO3_IO19	SAI5_RXFS	Generic GPIO	Y	+3,3V
91	HDMI_TXN2	HDMI_TX2_N	-	N	-
92	GPIO3_IO20	SAI5_RXC	Generic GPIO	Y	+3,3V
93	HDMI_TXP2	HDMI_TX2_P	-	N	-
94	MIPI_CSI1_D0_P	MIPI_CSI1_D0_P	MIPI_CSI -(MIPI Camera Serial Interface)	N	-
95	NC	-	-	-	-
96	MIPI_CSI1_D0_N	MIPI_CSI1_D0_N	MIPI_CSI - (MIPI Camera Serial Interface)	N	-
97	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P	MIPI_CSI - (MIPI Camera Serial Interface)	N	-
98	MIPI_CSI1_D3_P	MIPI_CSI1_D3_P	MIPI_CSI - (MIPI Camera Serial Interface)	N	-
99	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N	MIPI_CSI - (MIPI Camera Serial Interface)	N	-
100	MIPI_CSI1_D3_N	MIPI_CSI1_D3_N	MIPI_CSI - (MIPI Camera Serial Interface)	N	-
101	MIPI_CSI1_D2_P	MIPI_CSI1_D2_P	MIPI_CSI - (MIPI Camera Serial Interface)	N	-
102	MIPI_CSI1_D1_P	MIPI_CSI1_D1_P	MIPI_CSI - (MIPI Camera Serial Interface)	N	-
103	MIPI_CSI1_D2_N	MIPI_CSI1_D2_N	MIPI_CSI - (MIPI Camera Serial Interface)	N	-
104	MIPI_CSI1_D1_N	MIPI_CSI1_D1_N	MIPI_CSI - (MIPI Camera Serial Interface)	N	-
105	UART3_CTS_OUT	SD1_STROBE	UART CTS signal (OUTPUT)	Y	+3,3V
106	UART3_RTS_IN	SD1_RESET_B	UART RTS signal (INPUT)	Y	+3,3V
107	GND	-	Power PIN	N	-
108	UART3_TXD	UART3_TXD	UART TXD signal	Y	+3,3V
109	UART3_RXD	UART3_RXD	UART RXD signal	Y	+3,3V
110	I2C3_SDA	I2C3_SDA	I2C SDA Signal	Y	+3,3V
111	I2C3_SCL	I2C3_SCL	I2C SCL Signal	Y	+3,3V
112	UART1_TXD	UART1_TXD	UART TX DATA signal	Y	+3,3V
113	UART1_RXD	UART1_RXD	UART RX DATA signal	Y	+3,3V
114	I2S_DIN	SAI3_RXD	I2S interface	Y	+3,3V
115	I2S_LRCLK	SAI3_TXFS	I2S interface	Y	+3,3V
116	UART2_TXD	UART2_TXD	UART TX DATA signal	Y	+3,3V

Pin	Name	Pin Name on I.MX8MP	Primary Function Description	GPIO Capable	Voltage
117	UART2_RXD	UART2_RXD	UART RX DATA signal	Y	+3,3V
118	CAN1_TX	SAI5_RXD1	CAN Bus 1 interface Signal	Y	+3,3V
119	CAN1_RX	SAI5_RXD2	CAN Bus 1 interface Signal	Y	+3,3V
120	CAN2_TX	SAI5_RXD3	CAN Bus 2 interface Signal	Y	+3,3V
121	CAN2_RX	SAI5_MCLK	CAN Bus 2 interface Signal	Y	+3,3V
122	I2S_DOUT	SAI3_TXD	I2S interface	Y	+3,3V
123	GND	-	Power PIN	N	-
124	I2S_SCLK	SAI3_TXC	I2S interface	Y	+3,3V
125	GPIO4_IO28	SAI3_RXFS	Generic GPIO	Y	+3,3V
126	NC	-	-	-	-
127	ETH_TXRXM_A	-	Fast Ethernet signal	-	-
128	nRESET		Reset signal	N	+3,3V
129	ETH_TXRXP_A	-	Fast Ethernet signal	-	-
130	GPIO4_IO29	SAI3_RXC	Generic GPIO	Y	-
131	ETH_TXRXM_B	-	Fast Ethernet signal	-	-
132	PWM2_OUT	GPIO1_IO11	Generic PWM	Y	+3,3V
133	ETH_TXRXP_B	-	Fast Ethernet signal	-	-
134	+3V3_OUT	-	Output Power PIN	N	-
135	+3V3_OUT	-	Output Power PIN	N	-
136	MIPI_CSI2_D3_P	MIPI_CSI2_D3_P	-	-	-
137	ETH_nLINK	-	Link/Activity LED	-	-
138	MIPI_CSI2_D3_N	MIPI_CSI2_D3_N	-	-	-
139	ETH_nACT	-	Link/Activity LED	-	-
140	+3V3_OUT	-	Output Power PIN	-	-
141	ETH_TXRXM_C	-	Fast Ethernet signal	-	-
142	MIPI_CSI2_D2_P	MIPI_CSI2_D2_P	-	-	-
143	ETH_TXRXP_C	-	Fast Ethernet signal	-	-
144	MIPI_CSI2_D2_N	MIPI_CSI2_D2_N	-	-	-
145	ETH_TXRXM_D	-	Fast Ethernet signal	-	-
146	MIPI_CSI2_D1_P	MIPI_CSI2_D1_P	-	-	-
147	ETH_TXRXP_D	-	Fast Ethernet signal	-	-
148	MIPI_CSI2_D1_N	MIPI_CSI2_D1_N	-	-	-
149	MIPI_CSI2_D0_P	MIPI_CSI2_D0_P	-	-	-
150	GPIO3_IO21	SAI5_RXD0	-	Y	+3,3V
151	MIPI_CSI2_D0_N	MIPI_CSI2_D0_N	-	-	-
152	GPIO2_IO08	SD1_DATA6	-	Y	+3,3V
153	MIPI_CSI2_CLK_P	MIPI_CSI2_CLK_P	-	-	-
154	NC	-	-	-	-
155	MIPI_CSI2_CLK_N	MIPI_CSI2_CLK_N	-	-	-
156	GND	-	Power PIN	N	-

Pin	Name	Pin Name on I.MX8MP	Primary Function Description	GPIO Capable	Voltage
157	USB2_30_RXN	USB2_RX_N	-	-	-
158	USB1_30_RXN	USB1_RX_N	-	-	-
159	USB2_30_RXP	USB2_RX_P	-	-	-
160	USB1_30_RXP	USB1_RX_P	-	-	-
161	USB2_30_TXN	USB2_TX_N	-	-	-
162	USB1_30_TXN	USB1_TX_N	-	-	-
163	USB2_30_TXP	USB2_TX_P	-	-	-
164	USB1_30_TXP	USB1_TX_P	-	-	-
165	NC	-	-	-	-
166	SD0_B_DATA3	SD1_DATA3	uSDHC 2 DAT 3 signal	Y	+3,3V
167	SD0_B_CMD	SD1_CMD	uSDHC 2 CMD signal	Y	+3,3V
168	SD0_B_DATA0	SD1_DATA0	uSDHC 2 DAT 0 signal	Y	+3,3V
169	SD0_B_CLK	SD1_CLK	uSDHC 2 CLK signal	Y	+3,3V
170	SD0_B_DATA2	SD1_DATA2	uSDHC 2 DAT 2 signal	Y	+3,3V
171	SD0_B_DATA1	SD1_DATA1	uSDHC 2 DAT 1 signal	Y	+3,3V
172	GPIO2_IO06	SD1_DATA4	Generic GPIO	Y	+3,3V
173	JTAG_TRSTB	NC net to POR_B	JTAG Interface	N	-
174	JTAG_TDO	JTAG_TDO	JTAG Interface	N	+1,8V
175	JTAG_TDI	JTAG_TDI	JTAG Interface	N	+1,8V
176	JTAG_TMS	JTAG_TMS	JTAG Interface	N	+1,8V
177	JTAG_TCK	JTAG_TCK	JTAG Interface	N	+1,8V
178	GPIO2_IO07	SD1_DATA5	Generic GPIO	Y	+3,3V
179	GPIO2_IO20	SD2_WP	Generic GPIO	Y	+3,3V
180	NC	-	-	-	-
181	BOOT_MODE	-	Boot from USB/UART or Memory device	-	-
182	GND	-	Power PIN	N	-
183	SDIO_A_nCD	SD2_CD_B	uSDHC CD Signal	Y	+3,3V
184	GPIO1_IO01	GPIO1_IO01	uSDHC WP Signal	Y	+3,3V
185	SDIO_A_DATA2	SD2_DATA2	uSDHC DAT 2 signal	Y	+3,3V
186	SDIO_A_DATA3	SD2_DATA3	uSDHC DAT 3 signal	Y	+3,3V
187	SDIO_A_DATA1	SD2_DATA1	uSDHC DAT 1 signal	Y	+3,3V
188	SDIO_A_DATA0	SD2_DATA0	uSDHC DAT 0 signal	Y	+3,3V
189	SDIO_A_CLK	SD2_CLK	uSDHC CLK signal	Y	+3,3V
190	SDIO_A_CMD	SD2_CMD	uSDHC CMD signal	Y	+3,3V
191	USB1_ID	USB1_ID	USB on the go interface	N	-
192	USB1_DP	USB1_D_P	USB on the go interface	N	-
193	USB1_DN	USB1_D_N	USB on the go interface	N	-
194	USB2_DP	USB2_D_P	USB HOST interface	N	-
195	USB1_VBUS	USB1_VBUS	USB on the go interface	N	-
196	USB2_DN	USB2_D_N	USB HOST interface	N	-

Pin	Name	Pin Name on I.MX8MP	Primary Function Description	GPIO Capable	Voltage
197	+5Vin	-	Power PIN	N	-
198	+5Vin	-	Power PIN	N	-
199	+5Vin	-	Power PIN	N	-
200	+5Vin	-	Power PIN	N	-

Table 2

[1] *Connect to Coin-Cell or Super-Cap; left floating if not use*

The yellow rows highlight the required minimum electrical connections in order to make the module working correctly.

4.2 Electrical specifications

4.2.1 Operating Ranges

	V Min (Volts)	V Typ (Volts)	V Max (Volts)
Vin [1)]	-	+ 5	+ 5,25
VBUS_USB (180, 195)	-	+ 5	+ 5,25
GPIO V(oh)	+ 2,8	-	-
GPIO V(ol)	-	-	+ 0,4
GPIO V(ih)	+ 2,3		+ 3,3
GPIO V(il)	0	-	+ 0,6
GPIO V($oh_{1.8V}$)	+ 1,6	-	+ 1,8
GPIO V($ol_{1.8V}$)	-	-	+ 0,36
GPIO V($ih_{1.8V}$)	+ 1,25		+ 1,8
GPIO V($il_{1.8V}$)	0	-	+ 0,35

Table 3

[1)] This measure has done testing the module's start at the limit temperatures of -40°C and +85°C

4.2.2 Power Consumption

Module	Test condition	Current @ V Min	Current @ V Typ	Current @ V Max
i.Core MX8MP Quad	Linux Shell Running (no GUI)	-	-	-
	Linux Wayland Running	-	-	-
	Linux Wayland + WEBGL Running	-	-	-

Table 4

Chapter

5

5. Module Interfaces

This Chapter gives the technical specifications for carrier board design.

Section includes:

- ✔ **Power signals and backup battery**
- ✔ **Serials**
- ✔ **CAN Bus**
- ✔ **Ethernet**
- ✔ **USB**
- ✔ **SDIO**
- ✔ **LVDS**
- ✔ **HDMI**
- ✔ **MIPI DSI**
- ✔ **MIPI CSI**
- ✔ **PCIe**
- ✔ **Jtag interface**
- ✔ **Boot mode**
- ✔ **Touch screen controller**
- ✔ **Audio**
- ✔ **Reset pin management**

5.1 How to power the i.Core module

Read carefully the related sections before starting the power stage design. This module needs to be supply up to +5Vin power. Please refer to the table below for the power supply range specification. The power dissipated by the module in the operating mode is up to 600 mA, but **the system must provide at least a power of 2A at 5V to allow the start of the module.**

The following table shows the module power supply pins numbering, please connect all power supply pins in order to avoid damage.

Number	Name	Primary Function Description	GPIO Capable	Voltage
197	+5Vin	Power PIN	N	-
198	+5Vin	Power PIN	N	-
199	+5Vin	Power PIN	N	-
200	+5Vin	Power PIN	N	-
3	GND	Power PIN	N	-
4	GND	Power PIN	N	-
5	GND	Power PIN	N	-
22	GND	Power PIN	N	-
31	GND	Power PIN	N	-
39	GND	Power PIN	N	-
64	GND	Power PIN	N	-
71	GND	Power PIN	N	-
89	GND	Power PIN	N	-
107	GND	Power PIN	N	-
123	GND	Power PIN	N	-
156	GND	Power PIN	N	-
182	GND	Power PIN	N	-

Table 5

iMX8MP module has 5 Output power PIN usable for power source. The table below shows the power supply pins numbering.

Number	Name	Primary Function Description	GPIO Capable	Voltage
1	+1V8	Output Power PIN	N	-
2	+1V8	Output Power PIN	N	-
134	+3V3_OUT	Output Power PIN	N	-
135	+3V3_OUT	Output Power PIN	N	-
140	+3V3_OUT	Output Power PIN	N	-

Table 6

The following table shows the nominal maximum rating of power output:

Power output	Max output current
+1V8	200 mA (Total)
+3V3_OUT	600 mA (Total)

Table 7

WARNING!

The currents above 600 mA provided by the +3V3_OUT of the module, help to lower the performance in temperature.
We recommend adding a regulator voltage for an external current greater than or equal to 600 mA, in those applications where the operating temperature range is important.

For further details on the power supply refer to "i.MX8 MP" data sheet and Reference Manual.

5.1.1 How to connect a backup battery

The module allows the use of lithium rechargeable battery or supercapacitor as backup battery.
The connection with module is obtained by connecting directly the backup battery to the +Vcoin signal (pin 18 floating if not used).

Warning: the consumption of the RTC of the SOM is still under processing, an external RTC (on carrier board) may be the recommended solution.

Note: *The module is already designed to manage the charge of backup battery.*

5.2 How to connect two 3-wire RS232 serial port

This section shows how to use the iMX8MP UARTs as 3-wire RS232 serial ports. The table shows involved UARTs and the associated pins:

Number	Name	Primary Function Description	GPIO Capable	Voltage
112	UART1_TXD	UART1 TXD signal	Y	+3,3V
113	UART1_RXD	UART1 RXD signal	Y	+3,3V
116	UART2_TXD	UART2 TXD signal	Y	+3,3V
117	UART2_RXD	UART2 RXD signal	Y	+3,3V

Table 8

The signal on the module's UART pins are 3.3V logic level, this cannot be connected directly to a RS232 device like a PC Serial port, the use of a transceivers on the base board is mandatory in order to avoid module damage.

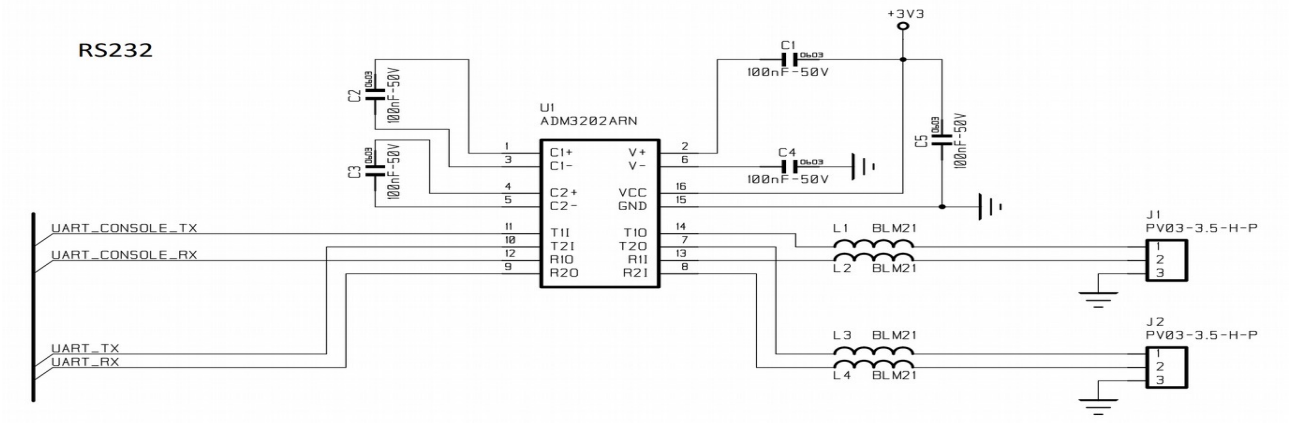


Figure 3

The figure shows how to connected the UART of the iMX8 using an RS232 transceiver. In the example an ADM3202ARN IC from Analog Device, is used like transceiver for both UARTs channels without any control signal. In case RTS and CTS are need, a transceiver must be used for these signals.

When Linux is installed on a module, UART2 is used like console. The default communications settings are shown in the table below.

Linux console default settings	
Baud rate	115200
Data length	8 bit
Parity	none
Stop	1bit

Table 9

* **Note**: in the i.Core MX8MP module *the UART2 is used as Linux Console*

5.3 How to connect a RS485 serial port

This chapter shows how an RS485 serial port can be connected to the module. The figure below shows how UART is connect to the RS485 transceiver.

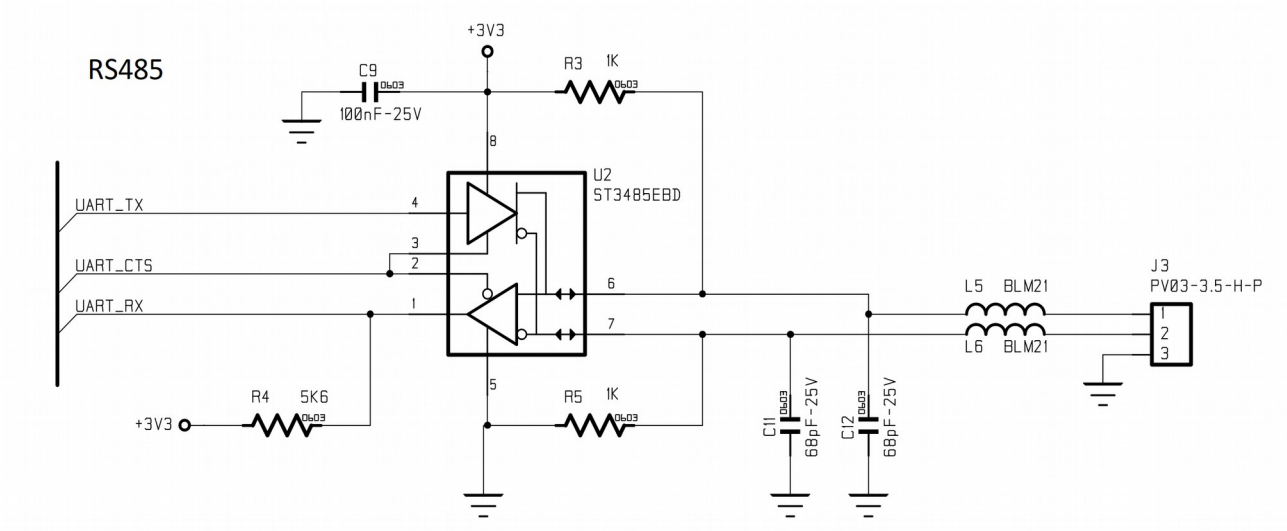


Figure 4

The pins involved in this RS485 communication in standard EDIMM spec are listed in the following table.

Number	Name	Primary Function Description	GPIO Capable	Voltage
105	UART3_CTS_OUT	UART3 CTS signal (Output)	Y	+3,3V
106	UART3_RTS_IN	UART3 RTS signal (Input)	Y	+3,3V
108	UART3_TXD	UART3 TXD signal (Output)	Y	+3,3V
109	UART3_RXD	UART3 RXD signal (Input)	Y	+3,3V

Table 10

5.4 How to connect CAN BUS interfaces

This chapter describes how CAN bus transceiver can be connected to the iMX8X module.

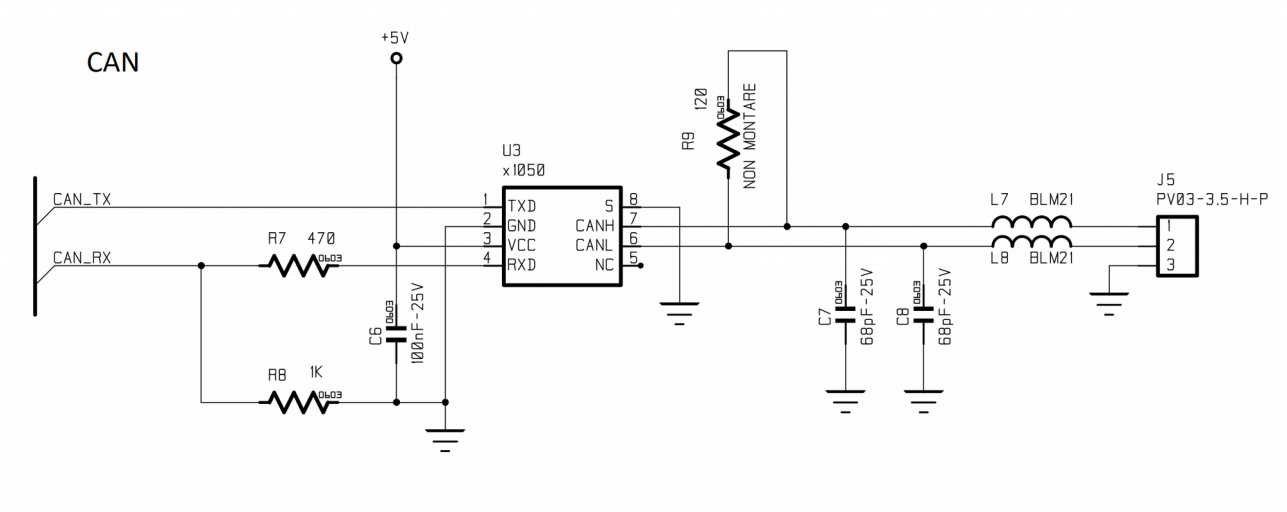


Figure 5

The following table describes the pins' numbering in the main connector involved in the CAN interface

Number	Name	Primary Function Description	GPIO Capable	Voltage
118	CAN0_TX	CAN 1 transmit signal	Y	+3,3V
119	CAN0_RX	CAN 1 receive signal	Y	+3,3V
120	CAN1_TX	CAN 2 transmit signal	Y	+3,3V
121	CAN1_RX	CAN 2 receive signal	Y	+3,3V

Table 14

Usually a Jumper is used to close the load of the CAN Bus to 120 Ω

5.5 How to design the Ethernet interface

The NXP iMX8MP Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE standard 802.3™ networks.

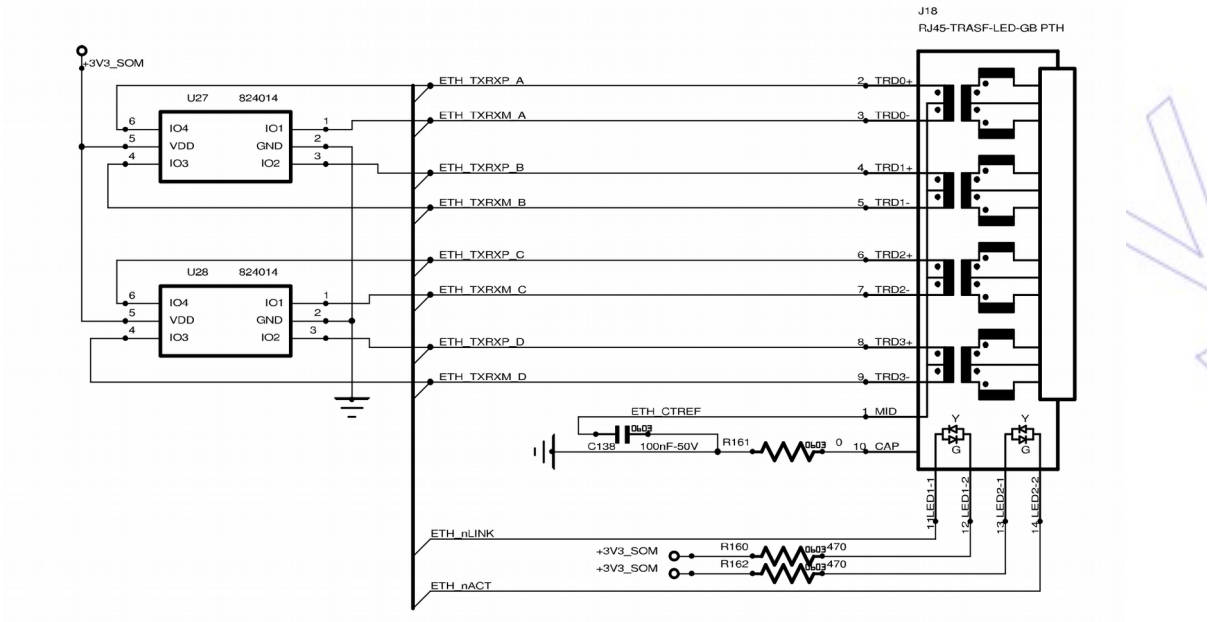


Figure 5

The table below lists all Ethernet signal of the module.
The primary function description is referred to the differential pair in 1000BASE-T mode.

Number	Name	Primary Function Description	GPIO Capable	Voltage
127	ETH_TXRXM_A	Positive transmit signal (TX-) for MDI configuration and the positive receive signal (RX-) for MDI-X configuration	-	+3,3V
129	ETH_TXRXP_A	Negative transmit signal (TX+) for MDI configuration and the negative receive signal (RX+) for MDI-X configuration	-	+3,3V
131	ETH_TXRXM_B	Positive receive signal (RX-) for MDI configuration and the positive transmit signal (TX-) for MDI-X configuration	-	+3,3V
133	ETH_TXRXP_B	Negative receive signal (RX+) for MDI configuration and the negative transmit signal (TX+) for MDI-X configuration	-	+3,3V
141	ETH_TXRXM_C [1)]	BI_DC- for MDI configuration and BI_DD+ for MDI-X configuration	-	+3,3V
143	ETH_TXRXP_C [1)]	BI_DC+ for MDI configuration and BI_DD– for MDI-X configuration	-	+3,3V
145	ETH_TXRXM_D [1)]	BI_DD- for MDI configuration and BI_DC+ for MDI-X configuration	-	+3,3V
147	ETH_TXRXP_D [1)]	BI_DD+ for MDI configuration and BI_DC– for MDI-X configuration	-	+3,3V
137	ETH_nLINK	Link/Activity LED	-	+3,3V
139	ETH_nACT	Link/Activity LED	-	+3,3V

Table 11

[1)] ***Note:*** In 10BASE-T/100BASE-TX these pin are not to be used

5.5.1 Component Placement considerations

Components placement can affect signal quality, emissions and can decrease EMI problems.

1. If the magnetics are a discrete component than the distance from the connector RJ45 should be kept to under 25mm of separation.
2. To decrease EMI problems the distance between magnetics and Phy should be at least 25mm or greater to isolate the PHY from magnetics.
3. The distance between Phy and RJ45 connector should always be within 200 mm.
4. The differential transmit pair should be keep at least 25mm from the edge of PCB up to the magnetics. If the magnetics are integrated into RJ45 the differential pair should be routed to the back of integrated magnetics RJ45 connector, away from the board of PCB.
5. The signals RX & TX should be independently matched in length to within 3 mm

See following figure

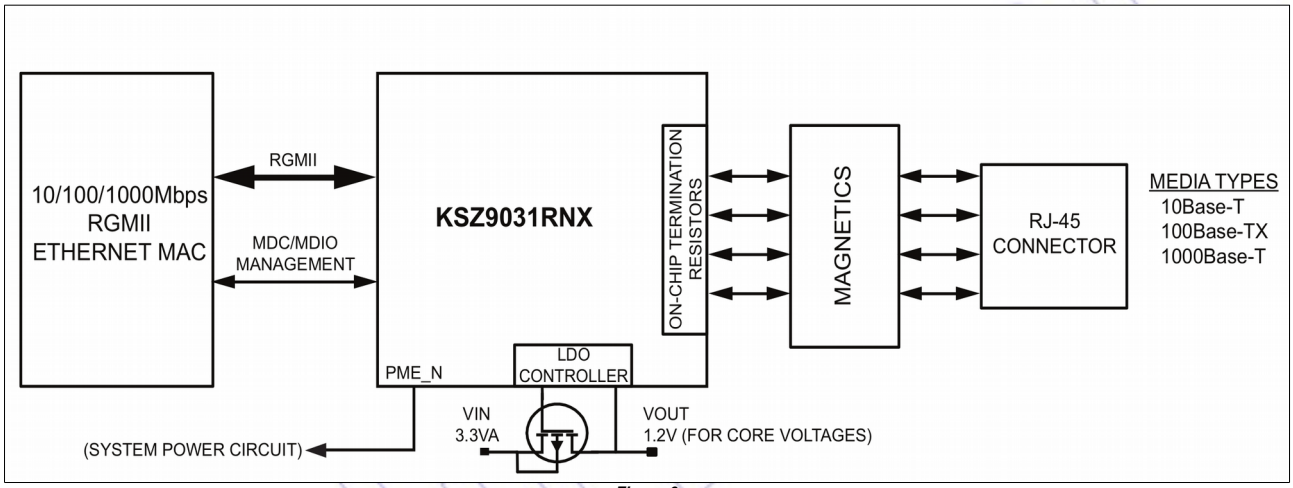


Figure 6

The PHY used in the module is the Microchip ***KSZ9031RNX***.
For more information refer to the Microchip Docs.

For a list of magnetics selected to operate with the ***KSZ9031RNX***, refer to the datasheet chapter: Magnetic – Connection and Selection**.**

*** figure from Microchip *KSZ9031RNX***

5.6 USB interface

5.6.1 How to connect the USB OTG interface

The NXP iMX8MP USB module provides high performance USB On-The-Go (up to 480Mbps), compatible with the USB 2.0 specification. An OTG HS PHY is also integrated so no external OTG PHY is needed on the baseboard. The figure shows how the MINI-AB USB/OTG connector is powered and connected in the evaluation board. The following table lists all USB/OTG signal of mail connector.

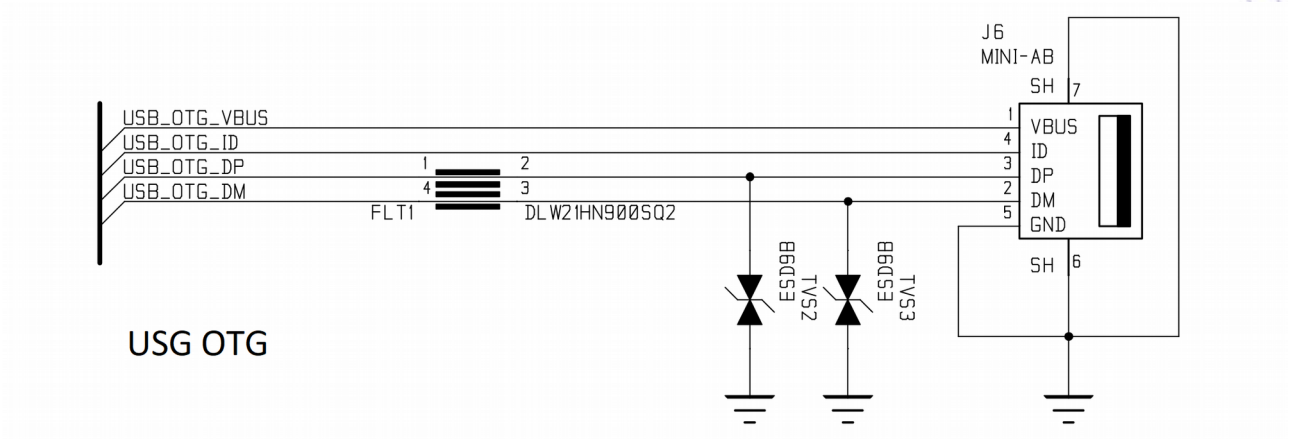


Figure 7

Number	Name	Primary Function Description	GPIO Capable	Voltage
195	USB1_VBUS *	USB on the go interface	N	-
192	USB1_DP	USB on the go interface	N	-
191	USB1_ID	USB on the go interface	N	-
193	USB1_DN	USB on the go interface	N	-

Table 12

**** Note: The USB_OTG_VBUS is an INPUT power signal. It must be connected to 5V***

The following figures show two different ways to connect the USB OTG interface that may be used to work as either a host or a device.

Use of the USB OTG port as a Host with its own dedicated supply. The ID signal is forced to GND

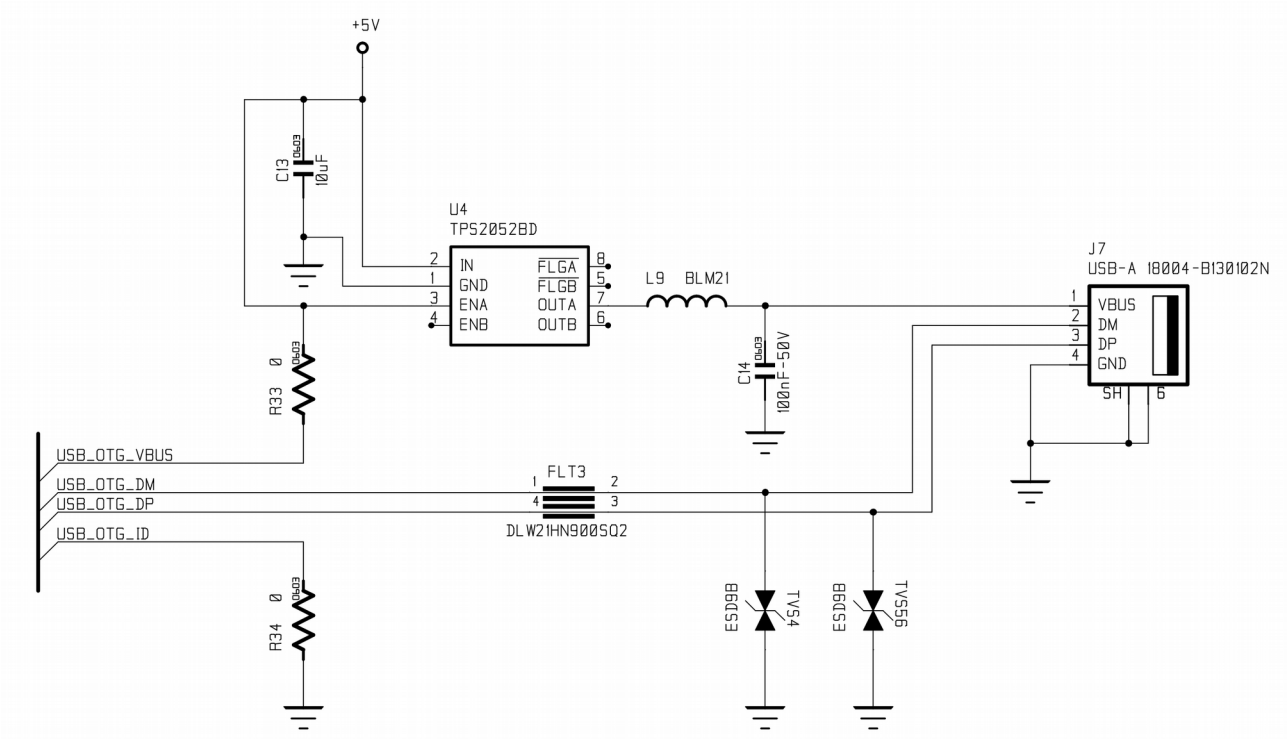


Figure 8

Use of the USB OTG port as Device or as Host depending on the status of the ID signal that is used also to enable the power supply.

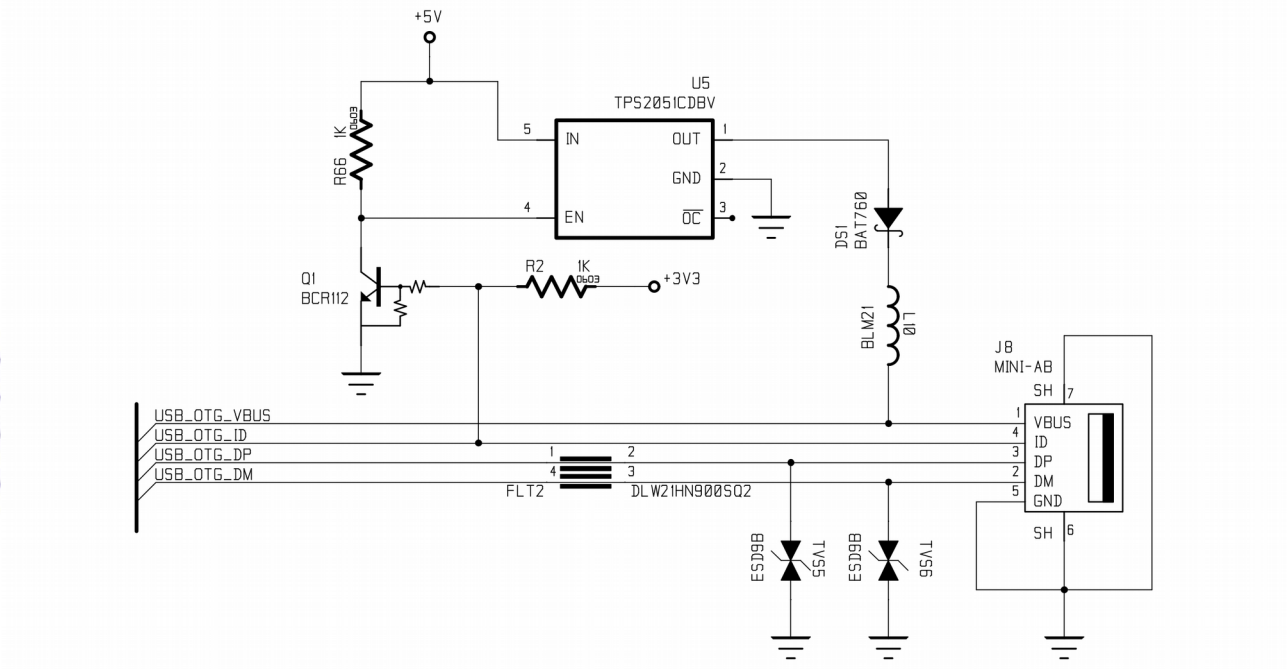


Figure 9

5.6.2 How to connect the USB host interface

The module provides one port for USB host interface. The figure shows how to connect this port to the Module.

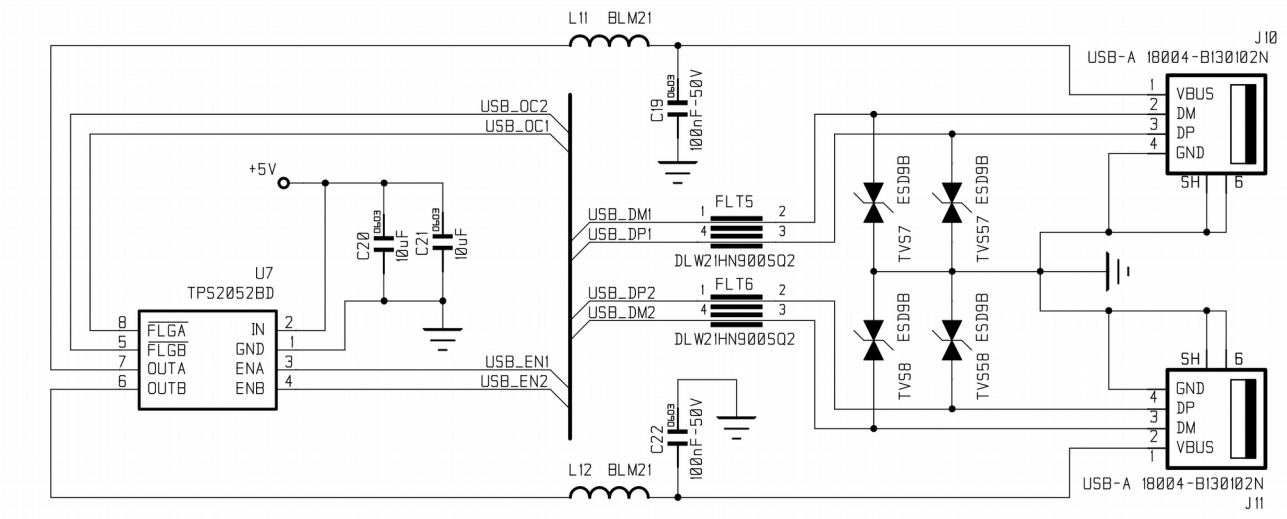


Figure 10

It's possible to multiply the USB ports available by equipping the carrier board with a USB HUB.

If only one port is needed it's possible to connect the USB_D (M/P) signals shown in the figure, directly to the module on pin 194-196 of the main connector.

Number	Name	Primary Function Description	GPIO Capable	Voltage
194	USB2_DP	USB HOST interface	N	-
196	USB2_DN	USB HOST interface	N	-

Table 13

* ***Note: The USB_H1_VBUS is an INPUT power signal. It must be connected to 5V***

5.6.3 USB 3.0 interface

USB 3.0 adds a SuperSpeed transfer mode, with associated backward compatible plugs, receptacles, and cables. SuperSpeed plugs and receptacles are identified with a distinct logo and blue inserts in standard format receptacles.

The SuperSpeed bus provides for a transfer mode at a nominal rate of 5.0 Gbit/s, in addition to the three existing transfer modes. Its efficiency is dependent on a number of factors including physical symbol encoding and link level overhead. At a 5 Gbit/s (625 MByte/s) signaling rate with 8b/10b encoding, the raw throughput is 500 MByte/s. When flow control, packet framing and protocol overhead are considered, it is realistic for 400 MByte/s (3.2 Gbit/s) or more to be delivered to an application

USB 3.0 combines USB 2.0 bus and new SuperSpeed bus with transfer rate up to 5.0 Gbit/s, which is about ten times faster than the USB 2.0 standard. USB 3.0 connectors are usually distinguished from their USB 2.0 counterparts by blue color-coding of the receptacles and plugs.

Below the map of additional superspeed signals

Number	Name	Primary Function Description	GPIO Capable	Voltage
158	USB1_RX_N	SuperSpeed receiver	N	-
160	USB1_RX_P	SuperSpeed receiver	N	-
162	USB1_TX_N	SuperSpeed transmitter	N	-
164	USB1_TX_P	SuperSpeed transmitter	N	-

Table 14

Number	Name	Primary Function Description	GPIO Capable	Voltage
157	USB2_RX_N	SuperSpeed receiver	N	-
159	USB2_RX_P	SuperSpeed receiver	N	-
161	USB2_TX_N	SuperSpeed transmitter	N	-
163	USB2_TX_P	SuperSpeed transmitter	N	-

Table 15

5.7 How to connect the SD CARD interface

The NXP iMX8MP Ultra Secured Digital Host Controller (uSDHC) provides the interface between the host system and MMC/SD/SDIO/CE-ATA cards, including cards with reduced size or mini cards. The module includes these features and the figure shows how the Micro SD Card connector is connected to iMX8MP Module in the evaluation board. The uSDHC signal of the module's main connector are listed in table below.

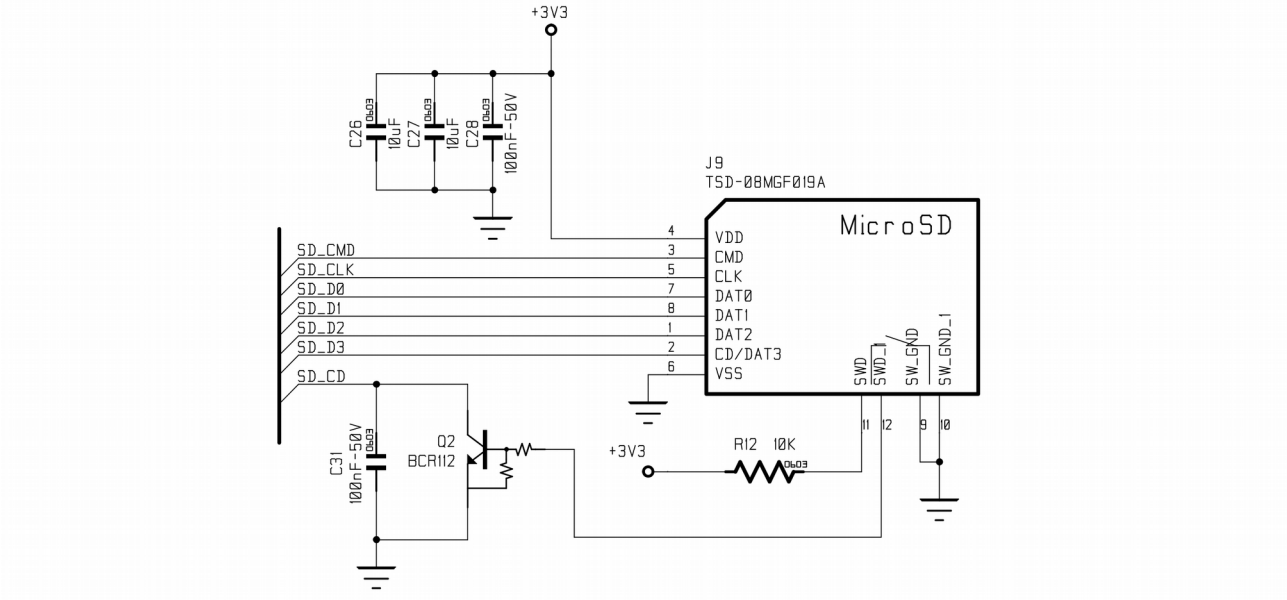


Figure 11

SDIO1 Interface

Number	Name	Primary Function Description	GPIO Capable	Voltage
183	SDIO_A_nCD	uSDHC CD Signal	Y	+3,3V
184	SD_WP (GPIO1_IO01)	uSDHC WP Signal	Y	+3,3V
188	SDIO_A_DATA0	uSDHC DAT 0 signal	Y	+3,3V
187	SDIO_A_DATA1	uSDHC DAT 1 signal	Y	+3,3V
185	SDIO_A_DATA2	uSDHC DAT 2 signal	Y	+3,3V
186	SDIO_A_DATA3	uSDHC DAT 3 signal	Y	+3,3V
189	SDIO_A_CLK	uSDHC CLK signal	Y	+3,3V
190	SDIO_A_CMD	uSDHC CMD signal	Y	+3,3V

Table 14

SDIO2 Interface

Number	Name	Primary Function Description	GPIO Capable	Voltage
37	SD2_nCD# (GPIO4_IO21)	uSDHC CD Signal	Y	+3,3V
35	SD2_WP (GPIO5_IO05)	uSDHC WP Signal	Y	+3,3V
166	SD0_B_DATA3	uSDHC 2 DAT 3 signal	Y	+3,3V
167	SD0_B_CMD	uSDHC 2 CMD signal	Y	+3,3V
168	SD0_B_DATA0	uSDHC 2 DAT 0 signal	Y	+3,3V
169	SD0_B_CLK	uSDHC 2 CLK signal	Y	+3,3V
170	SD0_B_DATA2	uSDHC 2 DAT 2 signal	Y	+3,3V
171	SD0_B_DATA1	uSDHC 2 DAT 1 signal	Y	+3,3V

Table 15

5.8 LVDS Interfaces

The i.Core MX8MP SOM is equipped with 2 LVDS interfaces, each interface has available up to 24 bit data connection. The LVDS ports may be used as follows:

- One single-channel output

Following the LVDS interfaces maps and schemes

Number	Name	Primary Function Description	GPIO Capable	Voltage
42	LVDS0_TX3_P	LVDS Interface's Signals	N	LVDS standard
44	LVDS0_TX3_N	LVDS Interface's Signals	N	LVDS standard
46	LVDS0_CLK_P	LVDS Interface's Signals	N	LVDS standard
48	LVDS0_CLK_N	LVDS Interface's Signals	N	LVDS standard
50	LVDS0_TX1_P	LVDS Interface's Signals	N	LVDS standard
52	LVDS0_TX1_N	LVDS Interface's Signals	N	LVDS standard
58	LVDS0_TX2_P	LVDS Interface's Signals	N	LVDS standard
59	LVDS0_TX0_P	LVDS Interface's Signals	N	LVDS standard
60	LVDS0_TX2_N	LVDS Interface's Signals	N	LVDS standard
61	LVDS0_TX0_N	LVDS Interface's Signals	N	LVDS standard

Table 16

Number	Name	Primary Function Description	GPIO Capable	Voltage
41	LVDS1_TX2_N	LVDS Interface's Signals	N	LVDS standard
43	LVDS1_TX2_P	LVDS Interface's Signals	N	LVDS standard
47	LVDS1_TX3_N	LVDS Interface's Signals	N	LVDS standard
49	LVDS1_TX3_P	LVDS Interface's Signals	N	LVDS standard
51	LVDS1_TX1_N	LVDS Interface's Signals	N	LVDS standard
53	LVDS1_TX1_P	LVDS Interface's Signals	N	LVDS standard
54	LVDS1_TX0_N	LVDS Interface's Signals	N	LVDS standard
55	LVDS1_CLK_N	LVDS Interface's Signals	N	LVDS standard
56	LVDS1_TX0_P	LVDS Interface's Signals	N	LVDS standard
57	LVDS1_CLK_P	LVDS Interface's Signals	N	LVDS standard

Table 17

The figure below shows a 24-bit LVDS port implementation, all the 3 channels are routed. We will refer to the channel by referring to the pairs signal “P” & “N”.

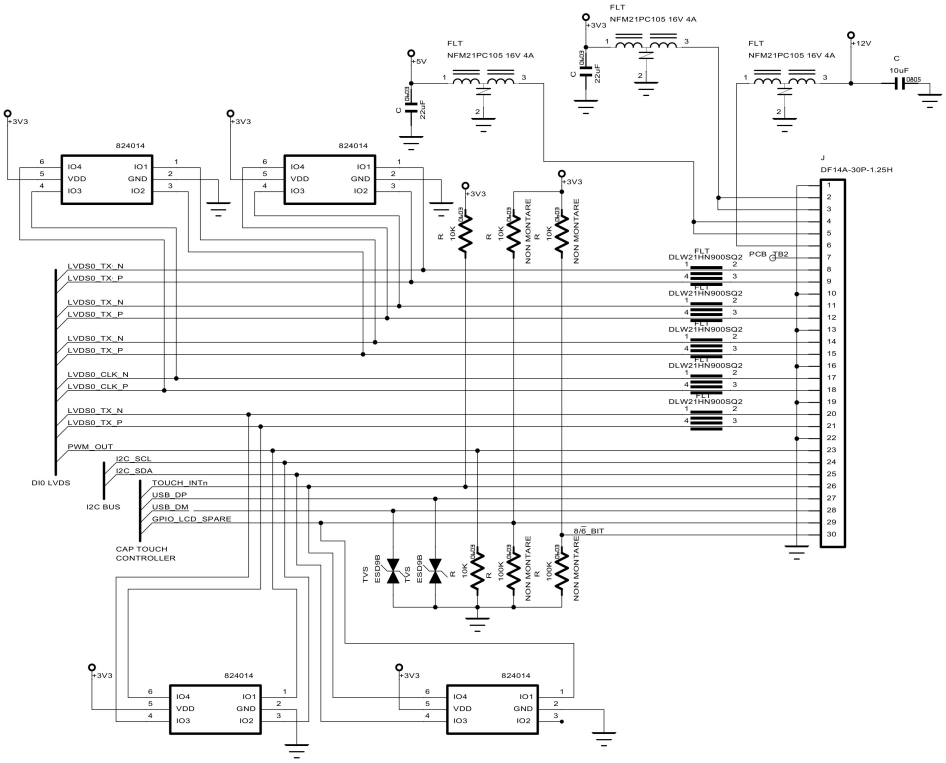


Figure 12

5.8.1 LVDS Routing and Placement Considerations

The LVDS lines are high-speed signals and as such during the designing must be complied with standards of protection against noise and crosstalk. In this chapter we give some advices about positioning, cabling and routing; for further details follow the guidelines and the manuals about LVDS bus.
Differential line: as mentioned we are working with fast signals, then to avoid disturbances and reduce noise on the line we suggest routing the channel lines in differential mode, for the same reason also the “channel” on the cable used to connect the board to TFT should be twisted.
Distance: there is no distance recommended between the devices but, always considering the nature of signals and that the driver is the same processor iMX8MP, we suggest to positioning the connector as close as possible to the module, and also to be aware to matching the line of differential pair as best as you can to avoid any kind of delay.
Controlled Impedance: all the signal's pairs must be traced in controlled impedance referred to the GND plane. This should avoid the problems due to reflections on the line. We suggest that the traces for LVDS signals should be closely-coupled and designed for 100Ω differential impedance.

Note: for further information consult differential micro-strips and high speed routing documentations

5.8.2 HDMI Interfaces

HDMI is capable of transferring uncompressed video, audio, and data using a single cable. The video pixel rates are typically from 25 MHz up to 297 MHz (4k x 2k and 3D video modes), but HDMI can support higher rates up to 340 MHz. It can support S/PDIF (IEC60958 L-PCM and IEC61937 compressed non-linear PCM: AC-3, MPEG-1/-2 Audio, DTS®, MPEG-2/-4 AAC, ATRAC, WMA, MAT) and Parallel HBR (high bit rate) audio interface, enabling the support of Dolby® True-HD and DTS-HD Master Audio. HDMI has the capability of automatically setting the display format configuration (intelligent link).

Number	Name	Primary Function Description	GPIO Capable	Voltage
70	HDMI_HPD	HDMI_HPD	N	-
73	HDMI_CEC	HDMI_CECIN	N	-
75	HDMI_CLKM	HDMI_CLKM	N	-
77	HDMI_CLKP	HDMI_CLKP	N	-
81	HDMI_TXN0	HDMI_D0M	N	-
83	HDMI_TXP0	HDMI_D0P	N	-
85	HDMI_TXN1	HDMI_D1M	N	-
87	HDMI_TXP1	HDMI_D1P	N	-
91	HDMI_TXN2	HDMI_D2M	N	-
93	HDMI_TXP2	HDMI_D2P	N	-

Table 21

The HDMI video out interface may be implemented as shown in the figure below.

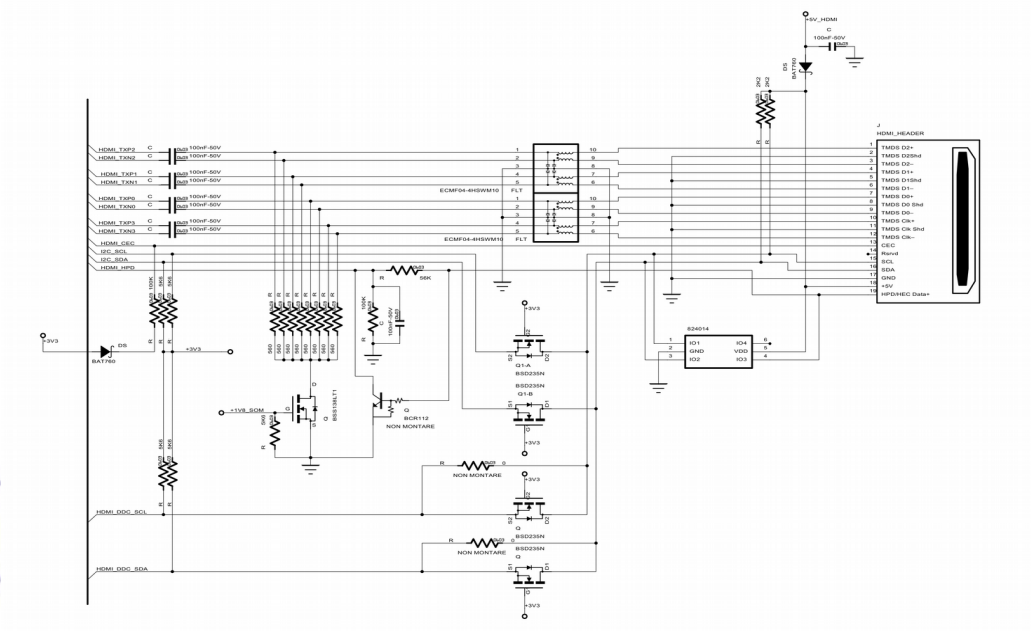


Figure 13

Note: for further details and applications refer to iMX8M RM document

5.9 MIPI DSI Interface

It's possible to bypass the MIPI CSI interface to connect an auxiliary MIPI DSI interface like video display output.

In this configuration, the pinout mapping of the SODIMM connector has to be considered as reported in the table

Number	Name	Primary Function Description	GPIO Capable	Voltage
136	MIPI_CSI2_D3_P	MIPI_DSI_D3_P	N	MIPI DSI standard
138	MIPI_CSI2_D3_N	MIPI_DSI_D3_N	N	MIPI DSI standard
142	MIPI_CSI2_D2_P	MIPI_DSI_D2_P	N	MIPI DSI standard
144	MIPI_CSI2_D2_N	MIPI_DSI_D2_N	N	MIPI DSI standard
146	MIPI_CSI2_D1_P	MIPI_DSI_D1_P	N	MIPI DSI standard
148	MIPI_CSI2_D1_N	MIPI_DSI_D1_N	N	MIPI DSI standard
149	MIPI_CSI2_D0_P	MIPI_DSI_D0_P	N	MIPI DSI standard
151	MIPI_CSI2_D0_N	MIPI_DSI_D0_N	N	MIPI DSI standard
153	MIPI_CSI2_CLK_P	MIPI_DSI_CLK_P	N	MIPI DSI standard
155	MIPI_CSI2_CLK_N	MIPI_DSI_CLK_N	N	MIPI DSI standard

Note: it's not possible to have both the Mipi-CSI2 and MIPI-DSI available at the same time. The standard assembly plan of the module provides the Mipi-CSI2 Interface.

5.10 MIPI CSI Interface

MIPI CSI interface is a specification of the Mobile Industries Processor Interface (MIPI) Alliance (see http://mipi.org for details)

The i.CoreM8 MP's equipped with 2 instances of MIPI CSI2 port. The CSI Receiver core can manage one clock lane and up to 4 data lanes through the lane management and de-packetization, providing a maximum throughput of 4 Gbps transfer rate.

Number	Name	Primary Function Description	GPIO Capable	Voltage
94	MIPI_CSI1_D0P	MIPI_CSI1 - (MIPI Camera Serial Interface)	N	-
96	MIPI_CSI1_D0N	MIPI_CSI1 - (MIPI Camera Serial Interface)	N	-
97	MIPI_CSI1_CLKP	MIPI_CSI1 - (MIPI Camera Serial Interface)	N	-
98	MIPI_CSI1_D3P	MIPI_CSI1 - (MIPI Camera Serial Interface)	N	-
99	MIPI_CSI1_CLKN	MIPI_CSI1 - (MIPI Camera Serial Interface)	N	-
100	MIPI_CSI1_D3N	MIPI_CSI1 - (MIPI Camera Serial Interface)	N	-
101	MIPI_CSI1_D2P	MIPI_CSI1 - (MIPI Camera Serial Interface)	N	-
102	MIPI_CSI1_D1P	MIPI_CSI1 - (MIPI Camera Serial Interface)	N	-
103	MIPI_CSI1_D2N	MIPI_CSI1 - (MIPI Camera Serial Interface)	N	-
104	MIPI_CSI1_D1N	MIPI_CSI1 - (MIPI Camera Serial Interface)	N	-

Table 18

Number	Name	Primary Function Description	GPIO Capable	Voltage
136	MIPI_CSI2_D3_P	MIPI_CSI2 - (MIPI Camera Serial Interface)	N	-
138	MIPI_CSI2_D3_N	MIPI_CSI2 - (MIPI Camera Serial Interface)	N	-
142	MIPI_CSI2_D2_P	MIPI_CSI2 - (MIPI Camera Serial Interface)	N	-
144	MIPI_CSI2_D2_N	MIPI_CSI2 - (MIPI Camera Serial Interface)	N	-
146	MIPI_CSI2_D1_P	MIPI_CSI2 - (MIPI Camera Serial Interface)	N	-
148	MIPI_CSI2_D1_N	MIPI_CSI2 - (MIPI Camera Serial Interface)	N	-
149	MIPI_CSI2_D0_P	MIPI_CSI2 - (MIPI Camera Serial Interface)	N	-
151	MIPI_CSI2_D0_N	MIPI_CSI2 - (MIPI Camera Serial Interface)	N	-
153	MIPI_CSI2_CLK_P	MIPI_CSI2 - (MIPI Camera Serial Interface)	N	-
155	MIPI_CSI2_CLK_N	MIPI_CSI2 - (MIPI Camera Serial Interface)	N	-

For further details and specifications refer to iMX8MP RM document

5.11 How to connect the PCIe interface

PCIe 2.0 PHY is a complete mixed-signal semiconductor intellectual property (IP) solution, designed for single-chip integration into computer applications. The PCIe2 PHY ssp_x1 includes all the necessary logical, geometric and physical design files to implement complete PCI Express 2.0 physical layer capability for 5Gb/s operation, connecting a host controller or device controller to a PCI Express system. This product is optimized for a system-on-Chip (SoC) design targeted to the TSMC 40LP1.1/2.5-V fabrication process.

The PCIe 2.0 PHY supports both the 5 Gbp/s data rate of the PCI Express Gen 2.0 specifications as well as being backwards compatible to the 2.5Gb/s Gen 1.1 specification.

Number	Name	Primary Function Description	GPIO Capable	Voltage
67	PCIE_RX_N	PCIe_RXN	N	-
69	PCIE_RX_P	PCIe_RXP	N	-
72	PCIE_TX_N	PCIe_TXN	N	-
74	PCIE_TX_P	PCIe_TXP	N	-
76	PCIE_REF_CLK_N	PCIe_REFCLKM	N	-
78	PCIE_REF_CLK_P	PCIe_REFCLKP	N	-

Table 19

It's strongly recommended to positioning the capacitor of PCIe signals as close as possible to the connector. Capacitors on RX signals may be unnecessary and replaceable with 0 Ohm resistors

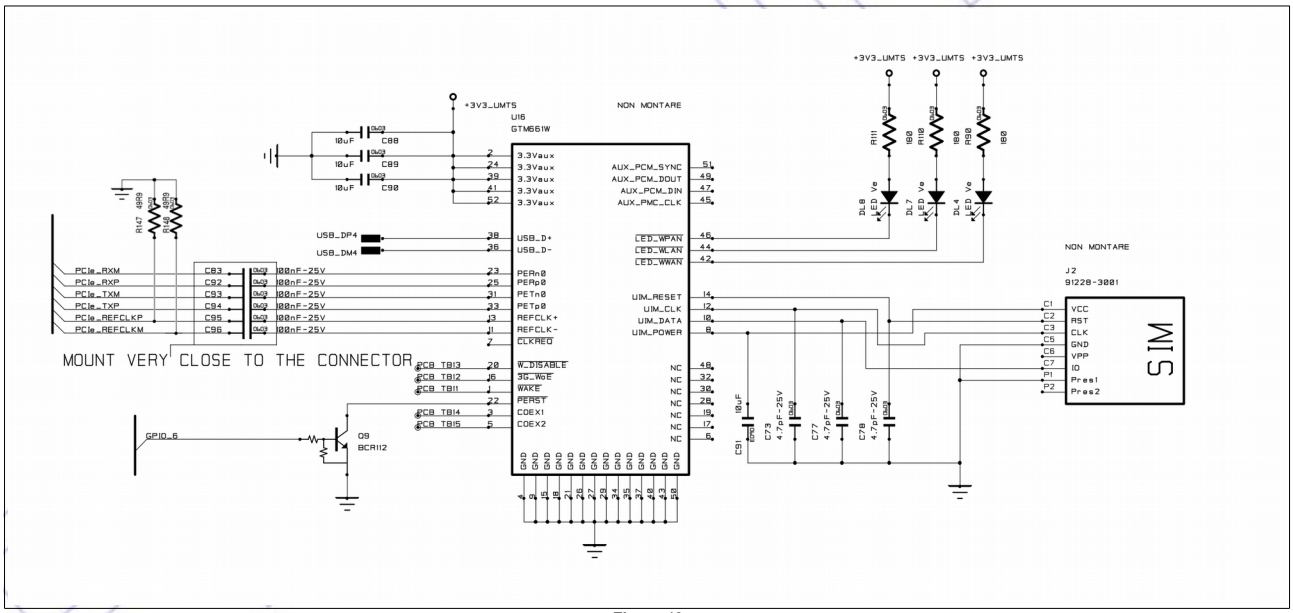


Figure 12

Termination is required on the differential clock lines. Connect two 49.9 Ω resistors, one between REFCLK- and GND, the other between REFCLK+ and GND. Alternately, Connect a 100 Ω resistor between REFCLK- and REFCLK+, as close as possible to the receiver device (connector).

Note: *for further details refer to PCIe recommendations on* ***iMX8MP*** *document (like design guide* ***iMX8MP*** *or reference manual).*

5.12 JTAG Interface

Joint Test Action Group (**JTAG**) is the common name used for the IEEE 1149.1 standard entitled **Standard Test Access Port and Boundary-Scan Architecture** for test access ports used for testing printed circuit boards using boundary scan. JTAG is often used as an IC debug or probing port.

There are no official standards for JTAG adapter physical connectors. Development boards usually include a header to support preferred development tools; in some cases, they include multiple such headers, because they need to support multiple such tools. For example, a micro-controller, FPGA, and ARM application processor will rarely share tools, so a development board using all of those components might have three or more headers. Production boards may omit the headers; or when space is tight, just provide JTAG signal access using test points.

The figure below shows how to connect a JTAG interface to iMX8MP Module.

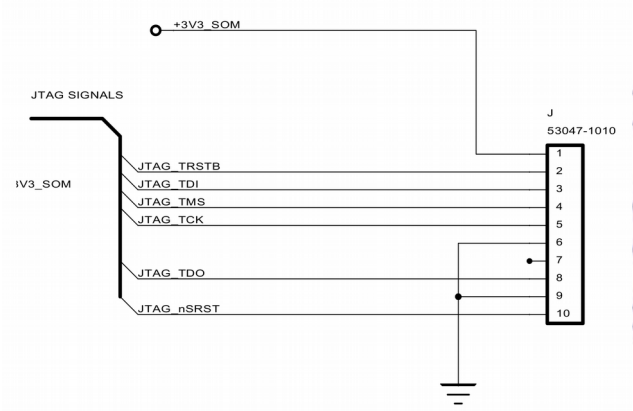


Figure 20

The table below lists all JTAG signals as mapped in the main connector.

Number	Name	Primary Function Description	GPIO Capable	Voltage
21	+1,8V	JTAG ref Voltage (Output Pin)	N	-
173	JTAG_TRSTB	JTAG Interface	N	+1,8V
174	JTAG_TDO	JTAG Interface	N	+1,8V
175	JTAG_TDI	JTAG Interface	N	+1,8V
176	JTAG_TMS	JTAG Interface	N	+1,8V
177	JTAG_TCK	JTAG Interface	N	+1,8V

Table 20

If you intend to use both module on your main board and don't use a JTag external console is mandatory to remove the pull-up/down resistors.

For further details refer to iMX8MP reference manual.

5.13 Boot Mode Pin

Boot mode pin determines how the module boot. The following table listed the possible options of the boot mode:

BOOT_MODE	Action
0	Boot from memory devices
1	Boot from Serial[1)]

Table 21

[1)] The boot from Serial is usually used for the boot loader deploy, for further information referring to the iMX RM.

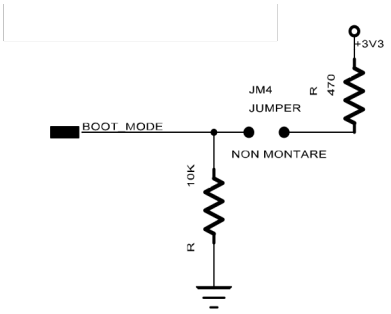


Figure 13

The table below lists the boot mode Pin numbering.

Number	Name	Primary Function Description	GPIO Capable	Voltage
181	BOOT_MODE	Boot from Serial or Memory device	N	-

Table 22

Following image shows the set-up configurations for bootstrap from eMMC and from SD card.

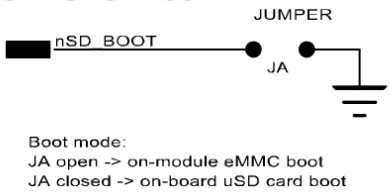


Figure 14

The signal used to configure the boot is implemented on pin 80. In the standard condition the signal is setting to boot from eMMC (jumper left open), closing the jumper the module start from SD card.
Following you can see the signals logical level to implement a custom starting sequence. The first sequence is already implemented in the module.

BOOT FROM Module's Memory Devices	
Signal on pin	LOGIC LEVEL
80	1

Table 23

The choice of boot from SD means short-cutting the jumper, you can have the same effect by pulling down directly the signal on pin 80.

BOOT FROM SD1	
Signal	LOGIC LEVEL
80	0

Table 24

Note: for using of any customized boot options refer to the NXP reference manual of iMX8MP

5.14 How to connect the Audio Interface

i.Core MX8MP is equipped with a SAI (Synchronous Audio Interface) that can be connected with a standard audio codec device.

The figure below shows connection with a Low Power Stereo Codec using the module signals interface

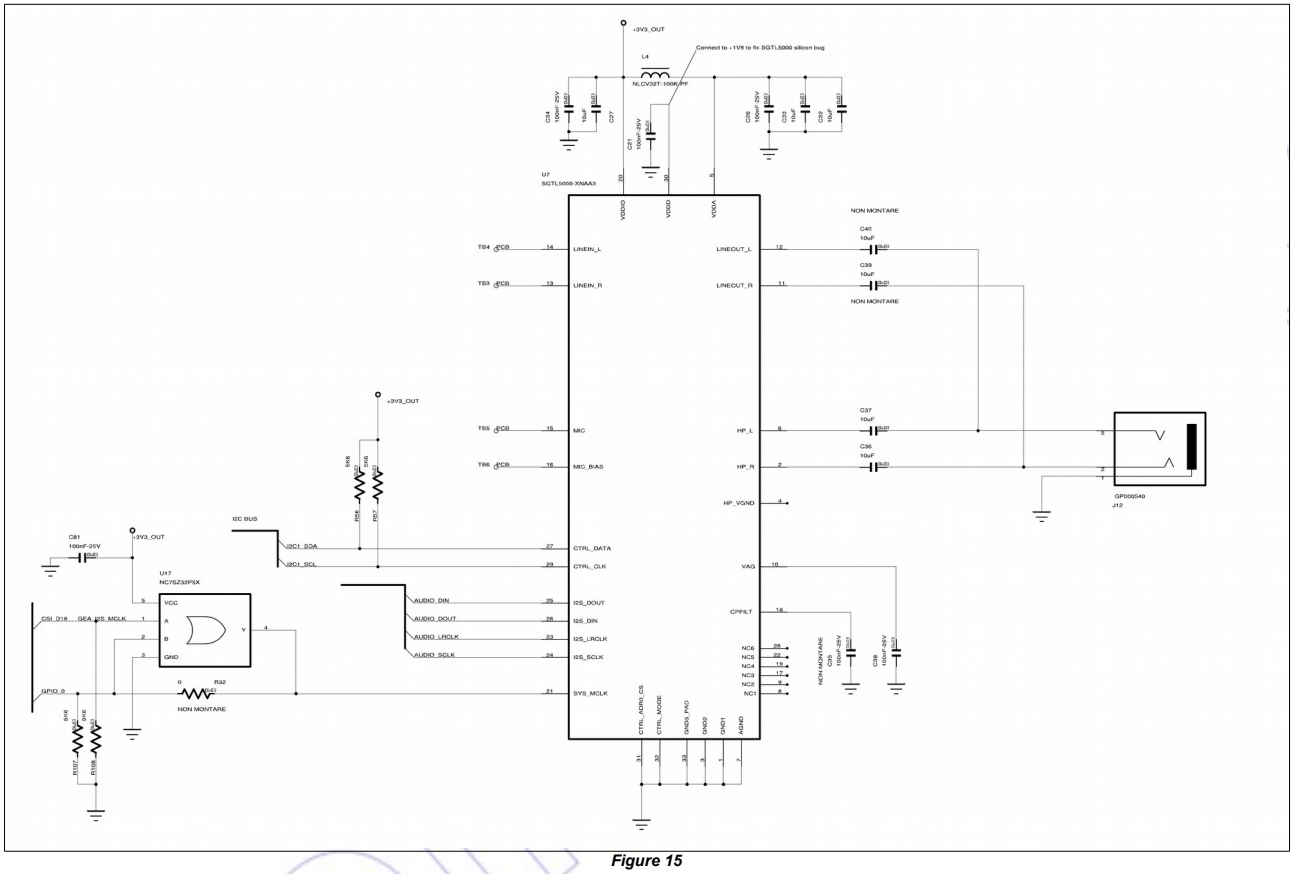


Figure 15

The following table lists the I2S BUS pins numbering

Number	Name	Primary Function Description	GPIO Capable	Voltage
114	I2S DIN	I2S Data In	Y	+3,3V
122	I2S_DOUT	I2S_Data OUT	Y	+3,3V
124	I2S_SCLK	I2S_SCLK	Y	+3,3V
115	I2S_LRCLK	I2S_LRCLK	Y	+3,3V

Table 25

WARNING!
To implement the SGTL5000 on the carrier board, remember to connect the VDD, pin 30 of the SGTL5000 device, to +1V8 to fix a silicon bug (for further detail refer to SGTL5000 data sheet)

5.15 How to connect the reset pin

The nRESET signal has input/output functionality and shall be driven in open-drain mode. *The signal has an internal 10K pull-up; the maximum recommended capacitive load is about **100pF**.*

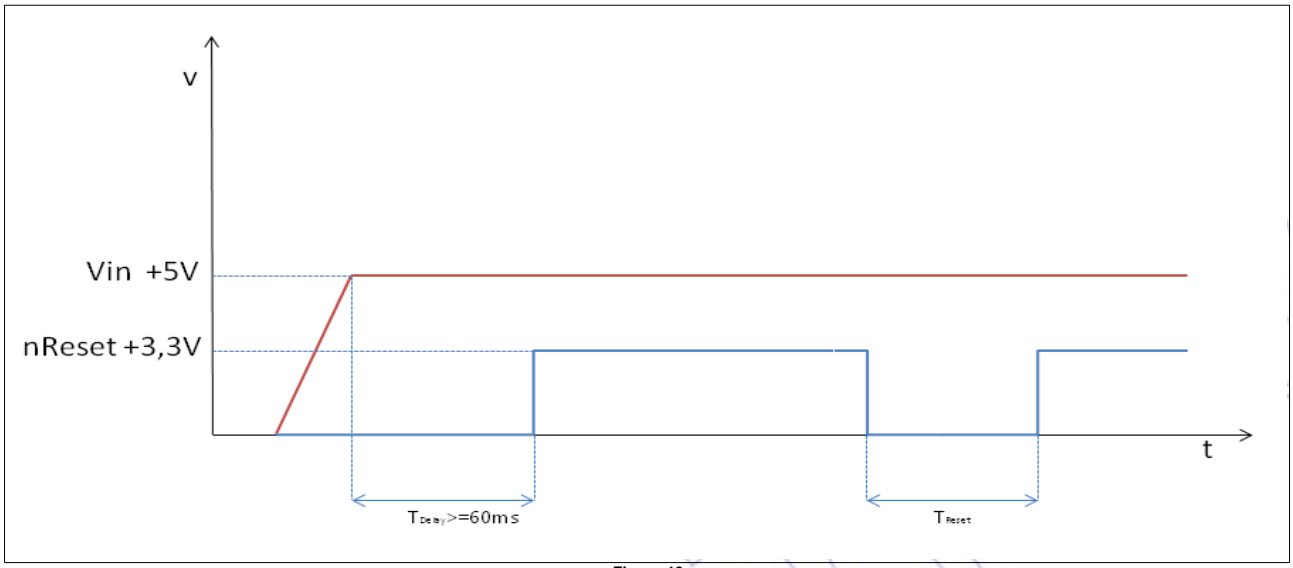


Figure 16

T_{Delay}: driven low by SOM during the POR state
T_{Reset}: driven low by user to force POR CPU pin

5.15.1 Input mode usage

The nRESET signal can be used to reset the module by driving it with an open-drain or with a simple button. If there are no special requirements, the module is fully auto-sufficient in terms of reset sequence, so its nRESET signal can be left floating. No Pull-up resistor is required on the carrier board; if a different pull-up resistor value (from the 10K on board of the module) is necessary, an additional pull-up on the carrier can be placed.

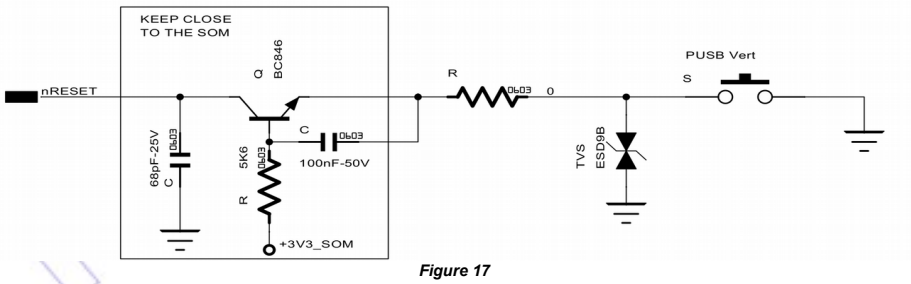


Figure 17

5.15.2 Output mode usage

The nRESET signal can also be used to monitor POR phase of the module, or to apply the reset (POR only) to other devices on the carrier. In this case, take care to always respect limits imposed by maximum capacitive load and minimum additional pull-up.

Note: in the i.Core MX8MP the nReset is not only a POR signal, it may driven by the SOM also during the CPU WDOG reset event.

Chapter

6

6. Peripheral multiplexing

This Chapter gives the alternative peripheral information

Section includes:

- ✔ **I2S**
- ✔ **SPI**
- ✔ **PWM**
- ✔ **GPT and I2C**
- ✔ **UART**
- ✔

6.1 Peripheral multiplexing description

In the following we describe opportunity to use alternative interfaces using the properties of multiplexing pin.
Refer to the NXP's reference manual and documentation for further details.

6.1.1 SPI & IIS Configuration

Using pin multiplexing 's features we may have the following SPI and IIS connections. The tables below show the output signals on the Connector's module.

ECSPI1 signals interfaces +3,3V

Pin number	Pin Name on I.MX8MP	Signal reference	Voltage reference
	ECSPI1_MOSI	MOSI	+3,3V
	ECSPI1_MISO	MISO	+3,3V
	ECSPI1_SCLK	SCK	+3,3V
	ECSPI1_SS0	SS0	+3,3V

Table 26

ECSPI2 signals interfaces +3,3V

Pin number	Pin Name on I.MX8MP	Signal reference	Voltage reference
	ECSPI2_MOSI	MOSI	+3,3V
	ECSPI2_MISO	MISO	+3,3V
	ECSPI2_SCLK	SCK	+3,3V
	ECSPI2_SS0	SS0	+3,3V

Table 27

The following tables show the pin configurations for IIS Bus on module's connector.

IIS2 bus interfaces

Pin number	Pin Name on I.MX8MP	Signal reference	Voltage reference
114	SAI3_RXD	I2S_DIN	+3,3V
122	SAI3_TXD	I2S_DOUT	+3,3V
124	SAI3_TXC	I2S_SCLK	+3,3V
115	SAI3_TXFS	I2S_LRCLK	+3,3V
34	SAI3_MCLK	I2S_MCLK	+3,3V

Table 28

IIS3 bus interfaces

Pin number	Pin Name on I.MX8MP	Signal reference	Voltage reference
	SAI2_RXD0	I2S_DIN	+3,3V
	SAI2_TXD0	I2S_DOUT	+3,3V
	SAI2_TXC	I2S_SCLK	+3,3V
	SAI2_TXFS	I2S_LRCLK	+3,3V

Table 29

6.1.2 Alternative PWM pins table

It's possible to set the pins shown in the following table as PWM signals.

Pin number	Pin Name on I.MX8MP	Signal reference	Voltage reference
		PWM-1	+3,3V
		PWM-1	+3,3V
		PWM-2	+3,3V
		PWM-3	+3,3V
		PWM-3	+3,3V
		PWM-4	+3,3V
		PWM-4	+3,3V
		PWM-4	+3,3V

Table 30

6.1.3 General Purpose Timer (GPT)

Using pin multiplexing 's features we may have the following GPT and IIC connections. The tables below show the output signals on the Connector's module.

GPT IN interfaces

Pin number	Pin Name on I.MX8MP	Signal reference	Voltage reference
		CAPTURE2	+3,3V

Table 31

GPT OUT interfaces

Pin number	Pin Name on I.MX8MP	Signal reference	Voltage reference
		COMPARE1	+3,3V
		COMPARE2	+3,3V
		COMPARE3	+3,3V

Table 32

GPT CLK interfaces

Pin number	Pin Name on I.MX8MP	Signal reference	Voltage reference
		GPT1 _CLK	+3,3V
		GPT2 _CLK	+3,3V
		GPT3 _CLK	+3,3V

Table 33

6.1.4 IIC Configuration

IIC2 interfaces

Pin number	Pin Name on I.MX8MP	Signal reference	Voltage reference
23	I2C2_SCL	SCL	+3,3V
24	I2C2_SDA	SDA	+3,3V

Table 34

IIC3 interfaces

Pin number	Pin Name on I.MX8MP	Signal reference	Voltage reference
111	I2C3_SCL	SCL	+3,3V
110	I2C3_SDA	SDA	+3,3V

Table 35

6.1.5 Alternative UART pins tables

The following tables show an alternative UART configuration

UART1 interfaces

Pin number	Pin Name on I.MX8MP	Signal reference	Voltage reference
	UART1_TXD	UART1_TXD	+3,3V
	UART1_RXD	UART1_RXD	+3,3V
	UART3_RXD	UART1_CTS_B	+3,3V
	UART3_TXD	UART1_RTS_B	+3,3V

Table 36

UART2 interfaces

Pin number	Pin Name on I.MX8MP	Signal reference	Voltage reference
		UART2_TXD	+3,3V
		UART2_RXD	+3,3V
		UART2_CTS_B	+3,3V
		UART2_RTS_B	+3,3V

Table 37

UART3 interfaces

Pin number	Pin Name on I.MX8MP	Signal reference	Voltage reference
		UART3_TXD	+3,3V
		UART3_RXD	+3,3V
		UART3_CTS	+3,3V
		UART3_RTS	+3,3V

Table 38

UART4 interfaces

Pin number	Pin Name on I.MX8MP	Signal reference	Voltage reference
		UART4_TXD	+3,3V
		UART4_RXD	+3,3V
		UART4_CTS	+3,3V
		UART4_RTS	+3,3V

Table 39

7. Carrier board recommended specifications

Following are the specifications required for the carrier board to avoid problems in the assembly process. The module is interfaced with the carrier board through a SO-DIMM with 200 positions connector type TYCO ELECTRONICS code 1473005-1 or compatible.
For proper assembly it is strongly recommended to paying attention to:

7.1 Planarity in finish process

Due to the technical and mechanical specifications of the connector we suggest the maximum planarity of the footprint on PCB, so we suggest a type of finish obtained by horizontal process (we suggest and use for our carrier boards a type Chemical Gold finish).

7.2 Planarity of PCB

Also, the planarity of the entire Printed Circuit Board must be kept in check especially when the carrier board grows in size. In this case we suggest you contact the manufacturer of PCB to understand how improve the planarity of ended board and optimize the process maintaining the electrical characteristics unchanged.

Note: for further detail refer to your SO-DIMM connector's data-sheet.

7.3 Power Supply

It's strongly recommended that the power supply of the carrier board, which feeds the driver and control devices connected with the iMX processor, begins to work after the initialization of the processor itself.

8. Product Compliance

In order to respect own internal policy regarding the environmental regulations and safety laws, Engicam in this chapter confirms the compliant, when applicable, of its own products to the normatives ROHS and REACH and to the recognized hazards.

No hazard to report!